ANALYSIS OF MULTI LEVEL DUAL BUCK INVERTER TOPOLOGY

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ABSTRACT—Three phase cascaded H-Bridge dual-buck inverter is presented in this paper, which is a new type of three-phase voltage source inverter (VSI). The proposed inverter does not need dead time, and thus avoids the shoot-through problems of traditional VSIs, and leads to greatly enhanced system reliability. Though it is still a hard-switching inverter, the topology allows the use of power MOSFETs as the active devices instead of IGBTs typically employed by traditional hard switching VSIs. As a result, the inverter has the benefit of lower switching loss, and it can be designed at higher switching frequency to reduce current ripple and the size of passive components. A unified pulse width modulation (PWM) is introduced to reduce computational burden in real-time implementation. Different PWM methods were applied to a three-phase dual-buck inverter, including sinusoidal PWM (SPWM), space vector PWM (SVPWM) and discontinuous space vector PWM (DSVPWM). Three-phase dual-buck inverter and its control system has been designed and simulated under different dc bus voltage and modulation index conditions to verify the feasibility of the circuit, the effectiveness of the controller, and to compare the features of different PWMs.

Index Terms—Dual-Buck Inverter, Three-Phase Inverter, Unified PWM, Voltage Source Inverter (VSI).

1. INTRODUCTION

Among various multilevel voltage-source inverters, the most commonly used and commercially available ones are the neutral-point-clamped inverter, flying capacitor inverter, and cascade H-bridge inverter [1]–[4]. The cascade type inverters are capable of reaching higher output voltage level by using commercially standard lower voltage devices and components. They also feature a modular design concept which makes maintenance less burdensome. The cascade inverters are well suited for utility interface of various renewable energy sources, such as photovoltaic’s, fuel cells, battery energy storage, and electric vehicle drives, where separate dc sources naturally exist. However, because most current cascade inverters are based on a series connection of several single voltage source inverters (VSI) with two active devices in one leg, they suffer from shoot-through problems, the most dominating failure of VSI. The widely used standard three-phase voltage source inverter (VSI) has two active switches in one phase leg that present some common problems. First, dead time is needed between the two active switches of the same phase leg, which reduces the equivalent pulse width-modulated voltage, and leads to output waveform distortions and less energy transfer. Second, even with dead time, shoot-through is still the major killer of VSIs, especially at some fault conditions. Third, people cannot simply employ power MOSFETs because of the reverse recovery problems of the body diode [1]–[5]. In order to obtain the benefits of using MOSFETs, such as low switching loss, resistive conduction voltage drop, and fast switching speed that allows reduction of current ripple and the size of passive components, conventional approaches adopt soft switching tech- passive components, conventional approaches adopt soft-switching techniques [6]–[9]. However, soft-switching inverters require additional auxiliary switches, passive components, and more gate driving circuits, which reduces reliability and increases system cost and complexity. Conventional three-phase dual-buck inverter, shown in Fig. 1(a). It is hard-switching-based, but it can incorporate power MOSFETs as the active switches. The device count is the same as that of the standard three-phase VSI using insulated-gate-bipolar-junction-transistors (IGBTs). The idea of a three-phase dual-buck inverter originated from single-phase half-bridge and full-bridge dual-buck inverters [10]–[12]. It does not need dead time and has no shoot-through concerns. Because the body diode of the MOSFET never conducts, I can be hard-switched. The free-wheeling diodes can be chosen independently with fast reverse recovery features to minimize switching loss. Compared to single-phase dual-buck inverter, the three-phase counterpart does not have double-fundamental frequency ripple on the dc bus, and can be modulated with discontinuous space vector PWM (DSVPWM) to further reduce the switching losses and fully utilize the dc bus voltage.
In order to modulate the three-phase dual-buck inverter, a unified pulse width modulation is adopted [13]–[15]. Compared to traditional space vector PWM (SVPWM) sector calculations, this method has much less computational burden. Due to the unique operation principle of the three-phase dual-buck inverter, the unified PWM is modified to use the current reference to generate the required gate signals. Different PWM methods can be considered as special cases of the unified PWM technique, including sinusoidal PWM (SPWM), space vector PWM (SVPWM), and discontinuous space vector PWM (DSVPWM).

This paper first presents the basic operation principle of the proposed inverter. Second, it analyzes the specific unified PWM technique applied to the three-phase dual-buck inverter. Third, it introduces the closed-loop controller design with proportional-resonant (PR) and admittance compensation controllers. Simulation results under different dc bus voltage and duty cycle conditions to compare SPWM, SVPWM, and DSVPWM. Efficiency of different cases was measured and compared.

II. TOPOLOGY OF CASCaded H-BRIDGE DUAL BUCK INVERTER AND OPERATION PRINCIPLE

The single-unit dual buck inverter has two basic forms, dual Buck half-bridge inverter and dual buck full-bridge Inverter. The proposed cascaded H-Bridge dual buck inverter is shown in Fig. 1(b). This paper will focus on the analysis, design, and testing to demonstrate the feasibility and advantages of cascade H-Bridge dual buck inverters. Fig. 1(b) shows the Topology of proposed cascade H-Bridge dual buck inverter model and fig. 1(c) shows the internal model of H-Bridge for a particular phase. The paper first shows different topologies of the proposed cascade H-Bridge dual buck inverters and their operation principles.

The proposed three-phase dual-buck inverter has been shown in Fig. 1(b). Though it is a VSI, the PWMS for the active switches are determined by the phase output current. Fig. 2 shows the relation between the polarity of phase current and the operation of switches. Take phase A, for example, when \(i_A\) is positive, \(S1\) and \(D4\) are the conducting devices and when \(i_A\) is negative, \(S4\) and \(D1\) are the conducting devices. The same operation principle applies to phases B and C.

Fig. 3 shows the four switching states for phase A. It can clearly be seen that the body diodes of \(S1\) and \(S4\) never have the opportunity to conduct, which ensures the safe switching of power MOSFETs.

Since there is only one active switch per leg, shoot-through is no longer possible. Therefore, the reliability of the three-phase dual-buck inverter is much higher than with traditional VSIs. No dead time is needed because when \(S1\) operates, \(S4\) is always OFF and vice versa. The output waveforms are more sinusoidal and the energy is transferred more completely without the dead-time effect. Because the power MOSFET and diode can be selected independently, the system efficiency can be further improved. To minimize conduction loss, it is better to choose a power MOSFET with smaller on-resistance and a power diode with smaller forward voltage. To optimize the switching loss, a diode with fast reverse recovery capability is preferred.
Fig. 1. Three-phase dual buck VSI with MOSFETs
(a) Conventional model
(b) Proposed cascade H-Bridge dual buck inverter.
(c) H-Bridge structure of proposed model

Fig. 2. Phase current and conducting devices relation.

IV. PWM ANALYSIS

Even though MOSFETs are used for the three-phase dual buck inverter to cut down switching losses, it is still a hard switching VSI. Therefore, it is better to further reduce the switching loss by incorporating DSVPWM. At the same time, the dc bus voltage can be fully utilized by adopting SVPWM or DSVPWM rather than SPWM. Traditionally, the SVPWM methods [17]–[19] need to do trigonometric calculation and perform recombination of actual gating times, which is unfavorable for real-time implementation by a digital signal processor. Thanks to unified PWM methods [13]–[16], SVPWM and DSVPWM can be equivalently generated using triangle carrier comparison like SPWM, which greatly reduces computational burden.

Fig. 4 shows the unified PWM generation block diagram. The switch to which PWM is applied is selected based on the current reference polarity. The phase duty cycles $d_a$, $d_b$, and $d_c$ are provided by a closed-loop controller, which will be discussed in Section IV. The injected zero sequence duty cycle $d_{zs}$ is generated by the following equation [13]

$$d_{zs} = -[(1 - 2K_o) + K_o \cdot d_{\text{max}} + (1 - K_o) \cdot d_{\text{min}}]$$

(1)

where $d_{\text{max}} = \max (d_a, d_b, d_c)$ and $d_{\text{min}} = \min (d_a, d_b, d_c)$. 
Fig. 4. PWM generation block diagram.

$k_0$ is the PWM determination factor. Under this unified PWM scheme, when $k_0 = 0.5$, the output PWM is SVPWM; when $k_0$ follows the relation in (2), the output PWM is DSVPWM with non switching state at phase current 60° peak region.

$$
k_0 = 0 \quad j < 0

k_0 = 1 \quad j > 0

j = \max (i_{a_{ref}}, i_{b_{ref}}, i_{c_{ref}}) + \min (i_{a_{ref}}, i_{b_{ref}}, i_{c_{ref}})$$  \hspace{1cm} (2)

Fig. 5 shows the simulation results of PWM generation using the unified PWM scheme with phase duty cycles $d_a = d_b = d_c = 0.9$: (a) is SPWM with $d_z = 0$; (b) shows the SVPWM when $k_0 = 0.5$; (c) shows the DSVPWM when $k_0$ follows (2). For SPWM, the maximum phase duty cycle is 1; but, after injecting $d_z$, SVPWM and DSVPWM can boost the phase duty cycle up to 1.15, which means 15% more dc bus voltage utilization gain.

From Fig. 5, it is clear that in terms of switching loss, SPWM is almost the same as SVPWM. In contrast, DSVPWM can further decrease switching loss because each phase does not switch for a 60° interval when its absolute phase current is the largest among the three phase currents. In addition, from (1) and (2), it is clear that the calculation burden required to implement his unified PWM is very small.

V. DESIGN OF CLOSED-LOOP SYSTEM

In order to demonstrate the feasibility and advantages of the three-phase dual-buck inverter, the closed-loop control is derived and designed for a three-phase standalone system.

$$L_j = L_p \quad i_j > 0

i_j < 0 \hspace{1cm} (3)$$

Fig. 6 shows the average model of three-phase dual-buck inverter. $d_j (j = a, b, c)$ is the phase duty cycle, $L_f$ and $C_f$ are the filter inductor and capacitor, and $L_j$ is the output inductor of each phase.
Define $L = L_j + L_f$, and the following equation can be obtained from Fig. 6:

$$d_j(t) \cdot \frac{v_{dc}}{2} - v_j(t) = L \frac{di_j(t)}{dt} \tag{4}$$

Transform (4) to $s$ domain

$$i_j(s) = \frac{1}{sl} \left( d_j(s) \cdot \frac{v_{dc}}{2} - V_j(s) \right) \tag{5}$$

So the transfer functions from duty cycle $d_j$ to current $i_j$ and voltage $v_j$ to current $i_j$ are as follows:

$$G_{id}(s) = \frac{i_j(s)}{d_j(s)} = \frac{v_{dc}}{sL} \tag{6}$$

$$G_{iv}(s) = \frac{i_j(s)}{v_j(s)} = \frac{1}{sL} \tag{7}$$

Where $G_{id}(s)$ is the control-to-output transfer function and $G_{iv}(s)$ is an uncontrolled feed-forward term.

Fig. 7 shows the control block diagram of the three-phase dual-buck inverter operating at standalone mode. The control adopts the natural frame in a-b-c coordinates without the burden of transformation back and forth into rotational d-q coordinates for the digital signal processor [20]. Therefore, the control design needs high controller gain at the fundamental frequency. The closed-loop design adopts a two-loop concept, the inner current loop with a PI controller, $G_{pl}(s)$, to achieve fast dynamic response and enough damping and the outer voltage loop with a PR controller, $G_{pr}(s)$, to ensure a higher loop gain at the fundamental frequency [20–23]. In addition, the closed-loop control utilizes an admittance compensation controller, $G_{ac}(s)$. By introducing the admittance compensation controller, $G_{ac}(s)$, the undesirable term, $G_{iv}(s)$, can be cancelled out, smoothing zero current start-up and reducing current steady-state error.

The PR controller transfer function can be represented as follows:

$$G_{pr}(s) = k_p + \frac{2\omega_{uc}s}{s^2+2\omega_{uc}\omega_c^2} \tag{8}$$

For a 2.5 kW, 208VAC output inverter system, the following parameters are obtained through frequency domain design: $k_p = 0.02$, $kr = 12$, $\omega_c = 10$. The current loop controller is a simple P-controller; its design result is shown in (9). The admittance loop gain is shown in (10).

$$G_{pl}(s) = 0.05 \tag{9}$$

$$G_{ac}(s) = v_{dc/2} \tag{10}$$

GLPF(s) is second order low pass filter with cut-off frequency 5 kHz and a damping ratio 0.7.

After obtaining phase duty cycles $d_j$ from Fig. 7, the unified PWM scheme shown in Fig. 4 can be used to generate the desired PWM to drive all the active switches. It is true that there will be some difference between the reference current and the real current around the zero-crossing, especially under transient conditions. In the prototype discussed here, the current sensor is simply used to feedback the real current information.

It is not specifically designed to track the zero-crossing. Therefore, the authors believe that it is better to use the reference as the PWM control signal because it has more immunity to noise, and does not have the current ripple problems of the real current. Experimental tests have been conducted using the reference signal, which proved to be no problem for the control performance.

On the other hand, if the real current polarity information can be accurately sensed and determined near the zero-crossing point, it might be better to use that information to generate the PWM. In [26], a real current polarity detection circuit and algorithm are provided, and these could be adopted in the proposed topology.

Of course, this will increase the complexity of the sensing circuit and require more of the computational capacity of the digital controller.
VI. STUDY OF SIMULATION RESULTS

In order to prove the viability and merits of the proposed three phase cascaded H-Bridge dual-buck inverter and evaluate the unified PWM scheme, output inverter system in standalone operation was designed and tested. The switching frequency is 20 kHz. All the devices are rated at 600V. The passive components are selected as follows: \( L_p = L_n = 250 \mu H \), \( L_f = 1 \) mH, \( C_f = 2.4 \mu F \). The obtained cut-off frequency with the filters is 2.9 kHz. The load is variable resistive load bank.

The design rules for \( L_p \) (\( L_n \)) are provided below:

Rule No. 1: For standalone and grid-tie applications, \( L_p \) (\( L_n \)) can be designed based on the same rule that a conventional three-phase VSI follows. In this case, \( L_p \) (\( L_n \)) serves as the filter \( L_f \). It can be chosen based on the ripple current requirement of \( i_a \), \( i_b \), and \( i_c \), as well as the controller demand of filter cut frequency after selecting \( C_{uf} \).

If Rule No. 1 is followed, the total inductance will be twice that of conventional three-phase VSIs because there are six inductors instead of three. To solve this, one phase can share a common filter inductor \( L_f \), and the remaining inductances can serve as \( L_p \) (\( L_n \)).

This solution was implemented in the prototype discussed in this paper. \( L_f \) is allocated 1 mH, and the remaining inductance, 0.25 mH, is dedicated to \( L_p \) (\( L_n \)).

In this way, a total of \( 3 \) mH inductance \( (1.25 \text{ mH} \times 6 - (0.25 \text{ mH} \times 6 + 1 \text{ mH} \times 3)) \) can be saved compared to Rule No. 1.
The inductance is only increased by 0.25 mH per phase compared to conventional VSIs. However, Rule No. 2 leads to another question: What is the smallest that $L_p$ ($L_n$) can be? Besides filtering, one of the functions of $L_p$ ($L_n$) is to protect against shoot-through under fault conditions. As discussed in Section II, in normal operation, the proposed inverter totally eliminates shoot-through problems. However, under some fault conditions, the gating signals for $S_1$ and $S_4$ might be high at the same time.

Under this condition, $L_p$ and $L_n$ are inserted in the shoot-through path through the dc power supply, which will limit the $di/dt$ of the devices, and thus decrease the failure rate of the circuit and provide enough time for the protection circuit to shut down the system. Therefore, larger $L_p$ ($L_n$) leads to less failure under fault conditions. As a result, when determining the value for $L_p$ ($L_n$) there is a tradeoff between cut-down of total inductance and protection under fault conditions.

Rule No. 3: In motor drive applications, there is no need to put in filter inductors because the motor inductance serves as the filter. In this case, $L_p$ ($L_n$) can be a smaller value selected to protect against shoot-through under fault conditions as discussed in Rule No. 2.

For SPWM, the phase duty cycle can reach 1, while for SVPWM and DSVPWM the duty cycle can be extended to 1.15. Two duty cycle conditions are tested: one is 0.9 for SPWM, SVPWM, and DSVPWM; the other is 1.1 for SVPWM and DSVPWM. For the 0.9 duty cycle condition, the dc bus voltage is set at 380V. For the 1.1 duty cycle condition, the dc bus is lowered to 308V. Efficiency curves of different test conditions were measured and plotted.
Fig. 8 shows the phase a duty cycle at 0.9 and the PWM for the active switch that operates during the positive half-cycle of each phase. It matches the simulation results. The PWM signals for the negative half-cycle are shifted 180° for each phase.

Fig. 9 shows the relationship between $da$, $dan$ and the corresponding PWM when the duty cycle is 1.1. It can be seen that after injection of $d_zs$ for SVPWM and DSVPWM, $da$ can be $m$ larger than 1, which means further utilization of dc bus voltage. $iS4$ is the current through $S4$. It is clear that when $S1$ is switching during the positive half-cycle, $S4$ is OFF because the current through the switch is zero. When $S1$ is OFF during the negative half-cycle, $S4$ is operating based on the PWM pattern provided.

Fig. 10 shows three-phase output current and phase-to-neutral voltage waveforms for SPWM, SVPWM, and DSVPWM under dc bus voltage 380V with duty cycle 0.9. It is at the peak power condition (2.5 kW) with 120Vrms and 7Arms ac output of each phase. It can be seen that the change between PWM schemes can be achieved effortlessly with unified PWM by adjusting the injected $d_zs$ while the output characteristics remain the same.

Fig. 11 shows three-phase output current and voltage waveforms for SVPWM and DSVPWM under dc bus voltage 308V with duty cycle 1.1. It can be seen that the output voltage is still 120V, but the dc bus requirement is greatly reduced for these two SVPWM methods.

Fig. 12 shows positive half-cycle three-phase output current waveforms for SPWM, SVPWM, and DSVPWM under dc bus voltage 380V with duty cycle 0.9. It is the half-cycle current, unique to this topology, which ensures that only one active switch per phase works at any given time, eliminating the possibility of shoot-through.

Results with proposed cascaded h-bridge dual buck inverter:
Loss analysis of the proposed inverter against conventional inverter is provided below:

1) Active switch loss comparison. Because of reverse recovery problems with the MOSFET body diode, conventional VSIs have to use IGBTs when the dc bus voltage ranges from 300V to 600V. This proposed topology avoids conducting through the body diode, and that is the reason why high voltage power MOSFETs (600V to 900V, such as Cool MOS or MD Mesh series) can be employed. Conventional inverters use IGBTs, and the switching loss of IGBTs is much higher than that of MOSFETs for two major reasons. First, the switching speed of IGBTs is slower, so the overlap time of voltage and current during switching is longer and the overlap area is larger. Second, when IGBTs turn OFF, there is a large tail current which creates higher losses. The proposed inverter uses MOSFETs to reduce switching loss through its faster switching and lack of turn-off tail current. Because MOSFETs have a resistive conduction voltage drop while IGBTs have a fixed voltage drop, the conduction loss is reduced as well when using MOSFETs. When this topology is used in higher current applications, MOSFETs can be paralleled to reduce the resistive voltage drop and thus still obtain a lower conduction loss than IGBTs of the same current rating.

Applications with very high output current may require more MOSFETs than can be practically put in parallel. In that case, it is a good idea to adopt the hybrid-switch concept [9], building each active switch by placing...
MOSFETs in parallel with an IGBT. The MOSFETs conduct when current is low, and the IGBT takes over under high current conditions. The hybrid-switch might suffer from the tail current of the IGBT during high-current operation, but, compared to conventional VSIs, performance is still better in low-current regions because of the MOSFETs.

2) Diode loss comparison. Most conventional inverters use IGBT modules with anti parallel diodes. Most diodes paired with IGBTs are not designed to be fast switching diodes. When the diodes turn OFF, there are large reverse recovery losses. In contrast, the proposed topology allows the designer to pick a better free-wheeling diode. It is desirable to choose diodes with fast or ultrafast reverse recovery features to further cut down the switching losses, and, at the same time, diodes with lower voltage drops can be selected to reduce conduction losses.

3) Inductor loss comparison. When this topology is used in standalone and grid-tie applications where filter inductors are needed, the losses in the inductors are the same as the Losses in conventional VSIs. Even though the three-phase dual-buck inverter has more inductors than a conventional VSI, the loss is the same because Lp only works during the positive half-cycle, and Ln only works during the negative half-cycle. In motor drive applications, because Lp and Ln are small values, the associated losses are also small. The energy lost in the inductors is outweighed by the energy saved in the active switches.

Therefore, the overall efficiency of the proposed inverter is higher than that of traditional VSIs.

VI. CONCLUSION

A new three phase cascaded H-Bridge dual-buck inverter is presented. It has the advantage of utilizing power MOSFETs as active switches, and improves inverter reliability by eliminating the possibility of shoot-through and the need for dead-time. In order to reduce the computational load on the digital signal processor, unified PWM was analyzed and applied, including SPWM, SVPWM, and DSVPWM. To prove the effectiveness of the proposed topology and control scheme, a three-phase dual-buck inverter system operating at standalone mode has been designed and simulated. Different PWM methods were tested under different dc bus voltage and duty cycle conditions.

REFERENCES


