Fuzzy Logic Based Series Compensator Using Cascaded Transformers Coupled With Three-Phase Bridge Converters

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ABSTRACT- This paper introduces a multilevel series compensator (MSC) to compensate unwanted signals like voltage sag/swell, harmonic compensation, or reactive power compensation done by dynamic voltage restorer or series active power filter (Series APF) using Fuzzy Logic Controller (FLC). The design of a fuzzy logic system starts with a set of membership functions for each input and a set for each output. A set of rules is then applied to the membership functions to yield a "crisp" output value. By using MSC can improve the power quality of load under unbalance conditions in stiff system. The arrangement is based on three-phase bridge (TPB) converters connected by means of cascaded single-phase transformers. This arrangement allows the utilization of a solitary dclink. A speculation for K-arranges in which K-transformers are combined with K-TPB converters is displayed. The topology licenses creating a high number of levels in the voltage waveforms with a low number of intensity switches in correlation with a great topology. The staggered waveforms are produced by the converters through a reasonable heartbeat width adjustment (PWM) procedure that mulls over the transformer turns proportions. Particularity and basic support make the proposed MSC an appealing arrangement contrasted and some regular designs. Show, PWM system, and generally control are talked about in this paper. Recreation and trial results are introducedtoo.fuzzy logic controller gives improved dynamic response than PI controller.fuzzy logic controller gives efficient results

I INTRODUCTION

Distribution power systems are suffering hard impact in their power quality. This is due to the intensive use of nonlinear loads added with the growth of renewable energy sources. Such aspects have been leading electrical power system to poor power quality levels. Most common disturbances include: 1) harmonic voltages/currents; 2) voltages imbalances; 3) voltage sags/swells; 4) flickers; 5) transients; and 6) interruptions. Among them, voltage sags have been considered the most important power quality problem and have been attracting much attention in the literature [1]–[3]. To mitigate voltage disturbances at the grid, some custom power devices have been introduced and investigated. For instance, dynamic voltage restorer (DVR) [4], [5], series active power filter (Series-APF) [6], [7], and unified power quality conditioner (UPQC) [8], [9].

These three options satisfy the series voltage compensation criteria. However, each of them present particularities on their application field. UPQC is attractive to compensate both voltage and current disturbances by using series and shunt converters [10]. If the dc energy storage unit is not a critical issue for the compensator design, DVRs should be suitable due to short time operation feature. On the other hand, Series-APF can operate without a dc source connected in the dc-link for harmonic voltages compensations. In this case, the dc-link regulation strategy must be considered for a satisfactory operation. The series compensator (DVR or Series-APF) is commonly composed of the following: 1) injection transformers; 2) voltage source converter (VSC); 3) energy storage; 4) optional passive filters; and 5) protection circuits (e.g., bypass thyristors). The VSC-based on two-level (2L) topology is the most common solution used for low-voltagesystems.

However, for high-voltage levels (i.e., high- power applications), 2L-based converters have experienced limitations and difficulty to penetrate in this market. The cost associated for designing a 2L based compensator for more than 690 V_{rms} (according to IEC) makes this solution not feasible for high- voltage applications. In this context, the multilevel- based VSC technology has become the most mature and feasible solution for this type of applications [4]. Multilevel series compensators (MSCs) have been investigated in different aspects which make clear the fact that the multilevel converters ensure that voltage waveforms can be synthesized with lower harmonic content than 2L converters and also operate at a higher dc voltage.

Some multilevel configurations can be highlighted from the technical literature [4]. However, those configurations have some issues associated to the high number of dc-link capacitors, inherent in their topology. For instance, cascaded neutral point-clamped (NPC) and cascaded flying capacitor topologies have issues with unbalanced dc- link voltages and power sharing in eachcell.

A conventional DVR based on cascaded transformer coupled with H-bridge (HB) converters was presented in [4]. Usually, injection transformers are taken into consideration for the series voltage compensator design. In this way, the transformer turn

ratio associated with each transformer can be considered to improve the waveform quality of the output voltage generated by the compensator. This paper proposes a series compensator based on cascaded transformers coupled with three-phase Bridge (TPB) converters, as i_l lustrated in Fig. 1. Equivalent multilevel operation is achieved with reduced number of semiconductor devices in comparison with conventional HB.

The multilevel waveforms are generated by TPB converters through a suitable pulse width modulation (PWM) strategy associated with the transformer turns ratio. The modularity and simple maintenance make the proposed MSC an attractive solution in comparison with some conventional configurations. The model and control are ad dressed in this paper. Simulation and experimental results are presented too.

II PROPOSED MSC MODEL

The configuration depicted in Fig. 1 is generalized for K-stages (i.e., K-transformers and K-TPB converters). The converters legs are represented by K-power switches (i.e., q1j, q1j , q2j , q2j, . . ., andqK j) in which the subscript j is related to each phase (j = a, b, c). In addition, power switches q and q are complementary from each other. The switching states of all power switches are representedby

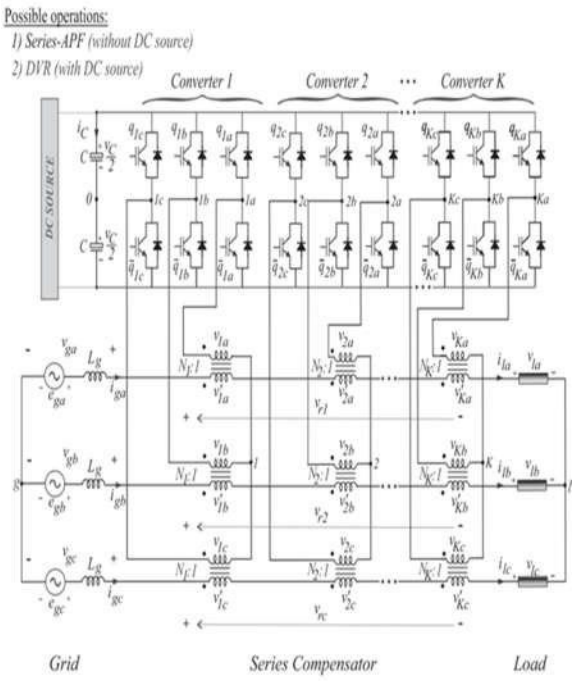


Fig. 1.Proposed MSC. Generalization with K-stages (i.e., K-cascaded transformers and K-TPB converters)

Binary variables, where q = 1 indicates a closed switch while q = 0 an open one. The configuration model becomes simple when its ideal equivalent circuit, see Fig.2, is considered. In this way, the converter pole voltages (v1j0, v2j0. . . vK j0), can be expressed as

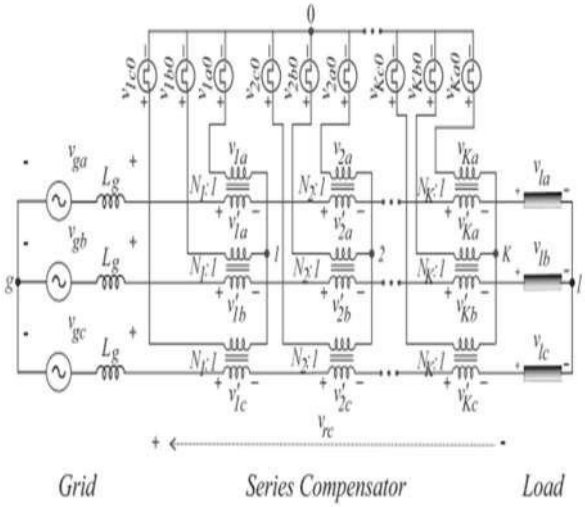


Fig. 2. Ideal equivalent circuit for generalization of the proposed MSC

$$v_{kj0} = (2q_{kj} - 1)\frac{v_C}{2} \quad (1)$$

where$k$correspondstoeachstage(i.e.,k=1,2,3,. . . ,K)and $v_C$is the dc-link voltage.

The voltages at the primary side of the injection transformers for each phase are expressed as

$$V_{ka} = V_{ka0} - V_{k0} \quad (2)$$
$$V_{kb} = V_{kb0} - V_{ko} \quad (3)$$
$$V_{kc} = V_{kc0} - V_{k0} \quad (4)$$

The system model considering the grid voltages (v_{gj}), trans former voltages at the secondary side (v1j, v2j. . . vK j) and load voltages (v_{lj}) can be expressed as

$$V_{gj} = (V'_{1j} + V'_{2j} + \cdots + V_{kj}) + V_{sj} - V_{gs} \quad (5)$$

where v1j = N1(v1j0 − v10), v2 j = N2(v2j0 − v20), .
. ., v K j = NK (vK j0 − vK 0) in which N1, N2, . . ., NK are the transformer turns ratios associated with converters 1, 2,..., K, respectively.

A simplified circuit can be obtained from the circuit depicted in Fig. 2 by considering perfect isolation from primary to secondary side of the transformers (i.e., ideal transformers), as shown in Fig. 3. Such an equivalent circuit permits to clarify the approach used to write the followingequations.

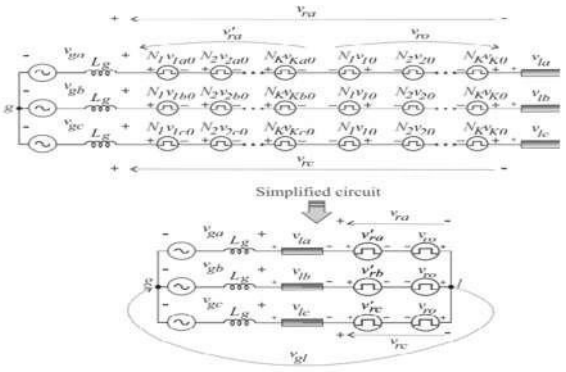


Fig. 3. Equivalent simplified circuit. Modified (on the top). Simplified (on the bottom).

It should be noticed that the output voltages (v_{rj}) of the resultant converter can be expressed as

$$V_{rj} = V_{rj} - V_{r0} \quad (6)$$

$$V_{rj} = N_1 v_{1j0} + N_2 v_{2j0} + \cdots + N_k v_{kj0} \quad (7)$$

$$V_{ro} = N_1 v_{10} + N_2 v_{20} + \cdots + N_k v_{k0} \quad (8)$$

From (8) and (5) the system model is simplified as

$$V_{gj} - V_{sj} = V''_{rj} = V'_{rj} - V_{ro} - V_{gs} \quad (9)$$

Voltages vrj can have a maximized number of levels if the voltages (vrj) assume a suitable sequence of the switching states. This is achieved by considering the transformer turns ratios (N1, N2, . . ., NK). Table I shows a particular case with three transformers per phase and three TPB converters, in which the voltage vrj can reach eight different levels per phase according to the switching states.

TABLE I

Variables for resultant converter with three cascaded transformers per phase and three TPB converters in which n1 = 1, n2 = 2, and n3 = 4

State	Leg state			Output voltage
	q_{3j}	q_{2j}	q_{1j}	$v'_{rj}=N_1v_{1j0}+N_2v_{2j0}+N_3v_{3j0}$
-7	0	0	0	$-7v_C/2$
-5	0	0	1	$-5v_C/2$
-3	0	1	0	$-3v_C/2$
-1	0	1	1	$-v_C/2$
1	1	0	0	$v_C/2$
3	1	0	1	$3v_C/2$
5	1	1	0	$5v_C/2$
7	1	1	1	$7v_C/2$

In this case, the compensator must operate with different transformer turns ratios (e.g., Nk = 2(k−1)). It can be seen that these ratios provide the best (higher) number of voltage levels, symmetrically spaced from each other. Fig. 4 presents an one-dimension region of output voltage vrj for each phase (e.g., j = a, b, c) associated with switching states [q1j, q2j, and q3j]. Such a representation permits to easily synthesize the reference output voltage by always using the switching states nearest to the reference output voltage.

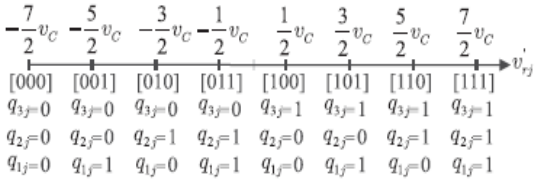


Fig. 4. One-dimension of output voltage (vrj) levels region for three-stages (i.e., K = 3 that means N1 = 1, N2 = 2, and N3 = 4).

This approach is similar to that one presented in and has advantages of reducing the switching losses of the converter topology. It is worth noting that either the order of the stages or transformers polarity can be modified to change the rated switching frequency in the legs with higher voltage or higher current. Table II shows the generalization for K-transformers and K-TPBconverters.

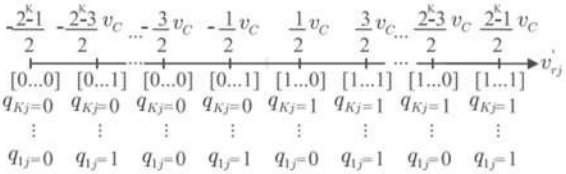


Fig. 5. One-dimension of output voltage (vrj) levels region for K-stages (i.e., that means N1 = 1, N2 = 2, N3 = 4, . . ., NK = 2(K −1)).

The respective levels disposition in one dimension region is presented in Fig. 5. Notice that the transformer turn ratios follow a geometric sequence with ratio equal to 2 (e.g., N1 = 1, N2 = 2, N3 = 4, N4 = 8, N5 = 16, . . ., NK = 2(K −1)) resulting always in the best option in terms of maximum number of levels generated at the voltage v rj and symmetrical dv/dt at vrj from one level to the other.

TABLE II

Variables for resultant converter with k-cascaded transformers per phase and k-TPB converters with nk= 2(k −1), valid for k ≥ 3

State	Leg state			Output voltage
	q_{Kj}	...	q_{1j}	$v'_{rj}=N_1v_{1j0}+N_2v_{2j0}+...+N_Kv_{Kj0}$
$-(2^K-1)$	0	...	0	$-(2^K-1)v_C/2$
$-(2^K-3)$	0	...	1	$-(2^K-3)v_C/2$
$-(2^K-5)$	0	...	0	$-(2^K-5)v_C/2$
⋮	⋮	⋯	⋮	⋮
-1	0	...	1	$-v_C/2$
1	1	...	0	$v_C/2$
⋮	⋮	...	⋮	⋮
2^K-5	1	...	1	$(2^K-5)v_C/2$
2^K-3	1	...	0	$(2^K-3)v_C/2$
2^K-1	1	...	1	$(2^K-1)v_C/2$

III PWM STRATEGY

The pulse width modulation (PWM) technique used in this work is the level-shifted-carrier-based PWM (LSPWM). Differently from conventional non sinusoidal carrier-based PWM (CPWM), a simpler algorithm calculation can be obtained. It takes into consideration references for the resultant output voltage (vrj∗). Considering that a voltage controller provides references for the resultant converter (vrj∗= (vgj − vlj)∗), the references $V^{*'}_{rj}$ become

$$V^{*'}_{rj} = V^{*''}_{rj} + V^{*}_{rog}$$

Fig. 6. PWM block diagram of generalized proposed MSC. Example of permissible levels were normalized by vC /2.

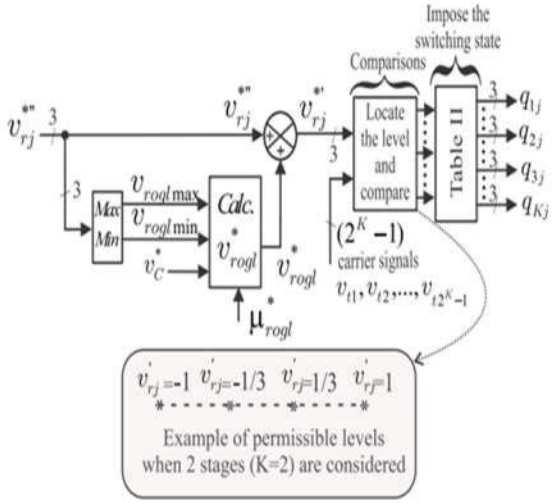
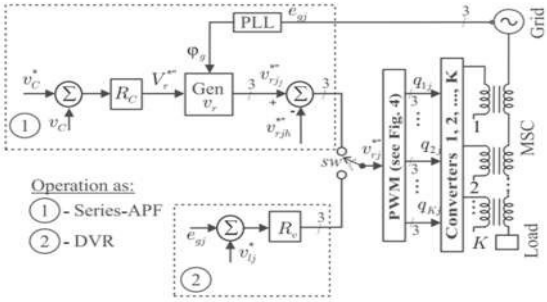


Fig. 7. Control block diagram of proposed MSC. Possible operations as a Series-APF (option 1) or as a DVR (option 2).

These small signals are subtracted from the harmonic voltage signals $v^{*''}$ to be compensatedIn this way, the reference voltages vrj∗ arecompared with $2^n - 1$ triangular waveforms, which are level-shifted carriers (vt1 to vt2n −1) placed according to the levels shown gives the switching states (q1j , q2j, . . ., qK j) that are imposed to each TPB converter. Fig. 6 summarizes each step of this PWM strategy.providing the voltages $v^{*''}$. More details about this control approach can be observed in [7]. In the second option, there is only controller Rv whose input sig nals are the grid voltages $v_{gj}$and reference loadvoltagesv_{Sj} Theoutputofcontroller Rvgives referencevoltagesv_{Sj} forthePWMstrategy.

IV CONTROL STRATEGY

Fig. 7 shows the control strategy of the proposed MSC. Notice that there are two options of operation: 1) as a harmonic Series-APF; or 2) as DVR. The first option regulates the dc-link voltage vC by means of a conventional proportional-integral (PI) controller. Such a controller is represented by the block RC which provides a small amplitude reference of the resultant voltage to be compensated $v^{*''}_{rjf}$. The block Gen − vr generates small reference voltages $v^{*''}_{rjh}$(at the fundamental frequency) synchronized with egj through the phase-locked-loop(PLL).



Asshown in Fig. 7, the switch SW indicates the selection of Series-APF or DVRoperation.

V COMPARISONS ANDANALYSIS

A. Number of Levels per PowerSwitch

This feature gives an idea of the cost-benefit associated with the studied topology. Assuming that the number of power switches are the same for both the proposed MSC and conventional HB converters

[4] configurations (i.e., four power switches per phase), the proposed MSC has K = 2 with trans former turns ratios N1 = 1 and N2 = 2 while the conventional HB has N1 = 1. It can be seen that proposed configuration presents a better performance if compared to conventional with HB, considering this characteristic. Hence, such an improvement is close to 33% (1/0.75) in the first case (with four power switches), while the second case (with eight power switches) is 76.99%(2/1.13). the proposedMSC that uses TPB converter for two different cases of load power (e.g., 40 and 275 kW). Additionally, it was considered the same number of power switches (i.e., six IGBTs) for both configurations. Additionally, the same WTHD (e.g., 0.21%) value was imposed to both of equal to 7.5 kHz. To obtain the same WTHD value, proposed configuration was operated with a frequency

decreased up to 3.3 kHz. Such a reduction can be observed via switching losses estimation. The normalized results of proposed topology in comparison with the conventional one are presented in Table V. It canbethem.

FUZZY LOGICCONTROLLER

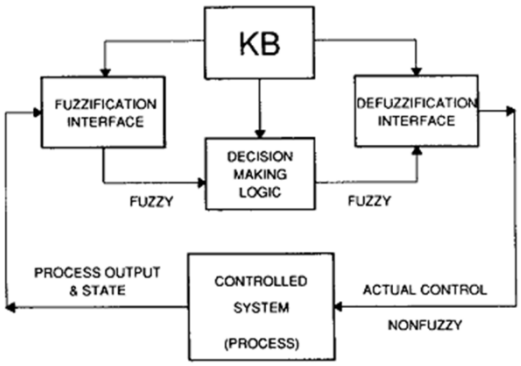


Fig. 8.Basic configuration of fuzzy logic controller (FLC).In this section, we present the main ideasunderlying the FLC.

1) The fuzzification interface involves the following functions:

a) Measures the values of inputvariables,

b) Performs a scale mapping that transfers the range of values of input variables into corresponding universes ofdiscourse,

c) Performs the function of fuzzification that converts input data into suitable linguistic values which may be viewed as labels of fuzzysets.

2) The knowledge base comprises knowledge of the application domain and the attendant control goals. It consists of a “data base” and a “linguistic (fuzzy) control rulebase:”

a) The data base provides necessary definitions, which are used to define linguistic control rules and fuzzy data manipulation in anFLC,

b) The rule base characterizes the control goals and control policy of the domain experts by means of a set of linguistic controlrules.

3) The decision making logic is the kernel of an FLC; it has the capability of simulating human decision- making based on fuzzy concepts and of inferring fuzzy control actions employing fuzzy implication and the rules of inference in fuzzylogic.

4) The Defuzzification interface performsthe following functions:

a) A scale mapping, which converts the rangeof values of output variables into corresponding universes ofdiscourse,

b) Defuzzification, Which yields a non-fuzzycontrol action from an inferred fuzzy controlaction

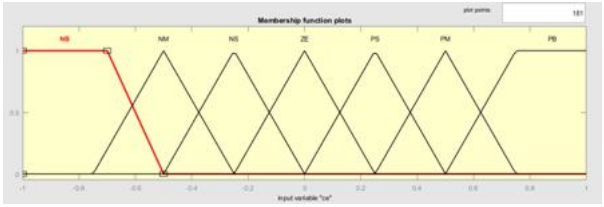


Figure 9: Error Input Membership Function

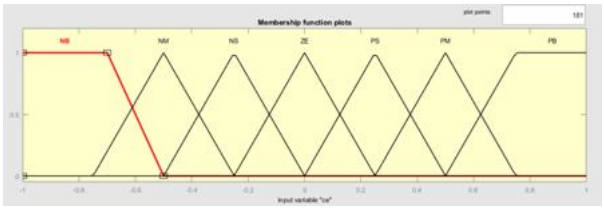


Figure 10:cumulative Error Input Membership Function

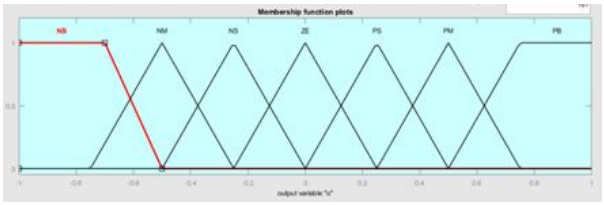


Figure 11: Output Membership Function

SIMULATIONRESULTS

Simulation results obtained from PSIM v9.0 are shown in Figs. 9 and 10. The dynamic operation of the MSC operating as a Series-APF and as a DVR has been verified. The implementation for this dynamic operation considering two options of operation (i.e., as a series-APF or as a DVR) was made through an equivalent single-phase configuration. In order to filter the high-frequency components provided by PWM converter, filtering capacitor and inductors (i.e., passive LCL filter) were connected in parallel with the transformers. Fig. 10 shows a steady state result in which the MSC is operating as a Series-APF. In this case, a fifth harmonic voltage was added in the fundamental voltageatthegrid$v_{ga} = V_g \sin(w_g t) + 0.2V_g \sin(5w_g t)$

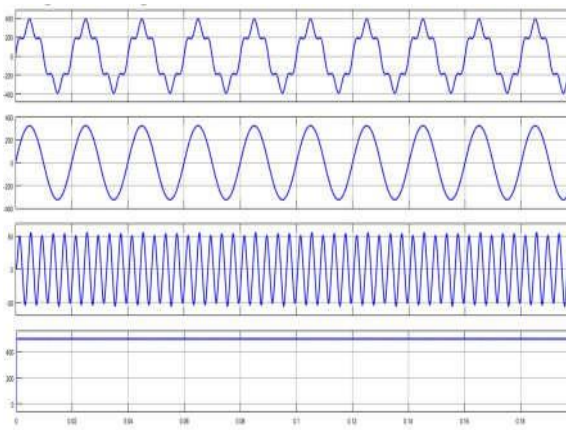


Fig. 9.Simulation result.MSC operating as a Series-APF. System voltages and the regulated dc-link voltage

The dc-link voltage (v_C) was regulated considering the control strategy described previously. It can be seen that disturbance is well compensated by the converter voltage (vra). The load voltage waveform (vla) was virtually sinusoidal. Fig. 10 shows MSC acting as a DVR. The compensator was tested under voltage sag. It can be seen that the voltage sag was compensated satisfactorily. To guarantee that the injected voltage was in phase with the grid, a PLL based on fictitious electrical power (i.e., power-based PLL) was considered. More details of this PLL can be foundin.

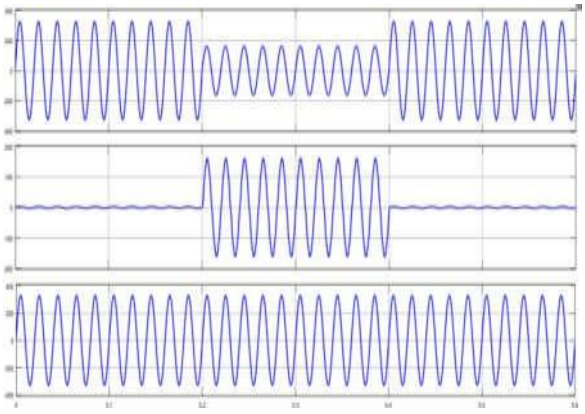
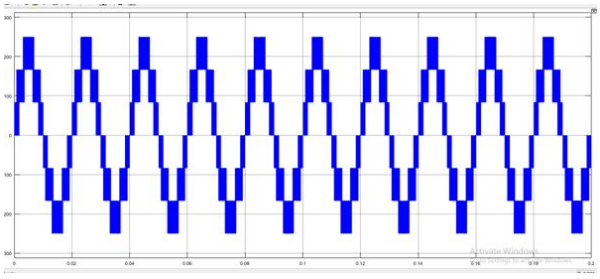
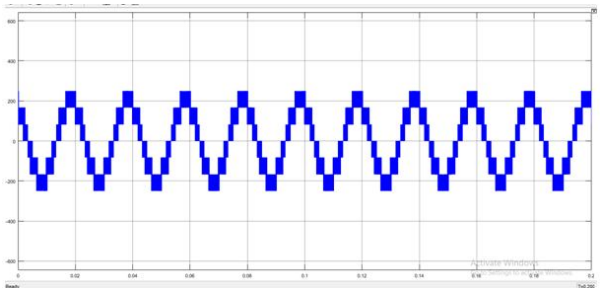


Fig. 10.Simulation result.MSC operating as a DVR. System voltages



(a)



(b)

Fig 11.Simulation results. Resultant phase-voltage (vr a) in phase a in which proposed MSC has two TPB converters. (a) Transformer turns ratios being equal to N1 = N2 = 1. (b) Transformer turns ratios being equal to N1 = 1 and N2 = 2.

V CONCLUSION

This paper has exhibited a MSC based on cascaded transformers combined with TPB converters. A speculation with K-stages was acquainted all together with demonstrate that by expanding the quantity of cells, the execution can be improved and additionally can build the power rating of the compensator. The arrangement is an attractive choice since it does not need with any extra dc-link capacitors as observed in some conventional multilevel compensator, for example, NPC, flying capacitors, cascaded HB, and so forth. SinceTPB modules are accessible in the market, the measured quality is a decent element for this topology. The proposed MSC has two choices of operation: 1) as a DVR; or 2) as a harmonic series active power filter (Series-APF). Some examination and correlations considering WTHD, semiconductor losses estimation and number of levels created per power switches were exhibited. Contrasted and conventional HB, the proposed MSC has displayed better qualities for these figures of merit. Simulation results were displayed with the end goal to approve hypothetical considerations.

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