DESIGN OF DIGITAL CIRCUIT BY USING ADPTIVE LOGIC

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ABSTRACT: Every digital circuit objective is to achieve MEP system i.e., minimum energy, minimum power, minimum voltage. These constraints can be achieved through adaptive logic. Adaptive logic is one of the fastest and innovative logic that has been implemented in digital circuit. Adaptive logic is implemented using the combination of both Nano magnetic technology and CMOS technology. Adaptive technique works very effectively in both threshold and sub – threshold regions. Internet - of - Things (IoT) is on the threshold of a massive breakthrough. Timing-error-detection (TED)-based systems is been shown to reduce power consumption or increase yield due to reduced margins. Reducing voltage in the circuit results in slow operation that incurs more delay. Generally delay is caused due to slow operation that results in error based upon the conditions. Canary circuit has been designed for error detection and error correction approach for reducing the power and voltage in a digital circuit. Canary circuit results in large delay. Adaptive logic, which is nothing but modified canary circuit with add-on components to canary circuit have been designed with dual latch phase in each stage. A combination of XNOR gate and flip-flop around each stage is added for the verification of correct operation. The entire architecture was modeled using Verilog code with the help of XILINX ISE tool.

LITERATURE SURVEY

For conventional synchronous systems operating at nominal voltages, a popular solution for overcoming margining has been to use canary circuit or replica circuits. Both are protective techniques, where the target is to track the delay of a real critical path with some added margin. The replica circuit can either be on the actual path or it can consist of a collection of digital gates with tunable delays. The latter is referred to as tunable replica circuit, and can be tuned on chip to match the delay of the critical path. In addition to global variations, the replica paths can track local dynamic voltage and temperature fluctuations if they are placed adjacent to the actual pipeline stages.

There are two approaches to overcome the limitation in the traditional design practices. One is to predict the occurrence of errors to avoid timing violation (error prediction approach), and the other is to detect actual errors and correct them (error detection approach). The error prediction approach uses sensors or canary circuits to monitor the magnitude of timing variations. On-chip measure the supply voltage or the temperature of the chip, and canary circuits measure the delay in critical path replicas of the chip. The error correction approach uses error detection sequential (EDS) circuits to detect the errors that actually occur and correct them using on-chip correction logic. Razoris a well-known EDS circuit, in which data are captured by a shadow latch with a delayed clock signal, as well as by a main flip-flop with a nominal clock.

Error correction methods:

If an error occurs at a particular stage, it is allowed to propagate until the last stage, and then all stages in the pipeline are flushed. If there are N pipeline stages, this will require N cycles. The failed instruction is then reissued to the pipeline, with the clock running at half speed, which should ensure that the failing instruction does not cause another error. This rerun takes 2N cycles, and so the completion time of the next instruction that follows the error is delayed by 3N cycles.

Bubble Razor represents a breakthrough, because it reduces the timing penalty to one cycle based on local stalling, allowing it to be used in complicated and high-frequency designs. However, unlike other methods, Bubble Razor can only be used for two-phase transparent latch-based designs.

Typical Case Design Methodology

In this methodology designer divide its design into two parts

1) Performance Oriented Design
2) Function Guaranteed Design

In Performance oriented design, designer has to think only about the typical cases and need not worry about worst possible cases. In function guaranteed design designer has to consider only about the function and not about the performance therefore all the worst cases possible will be included here.

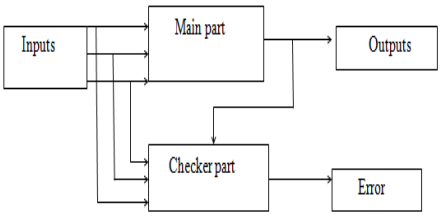

Figure 1: Typical case design methodologies

Razor logic contains a main flip-flop, shadow latch, XOR gate and mux. We use Razor flip-flops to detect operation that is considered to be a one-cycle pattern can really finish in a cycle. If not, the operation is re-executed with two cycles. Although the re-execution may seem costly, the overall cost is low because the re-execution frequency is low.

Proposed System:

The architecture of the proposed work composed of different individual modules are 3:1 Dickson DC-DC converter and TEP adaptive load which is composed of 5-Stage circuit with individual lower modules composed of clock control circuit, D-Latch, D-flip flop, EDS circuit ,EXOR gate. In each stage dual D-latch is used to reduce the delay. When TEP is integrated into a dual-phase latch pipeline, the resulting system cannot only tolerate late signals, but does not require additional hold buffers on fast paths. This is a large advantage compared with a traditional TED system.

Canary logic:

Razor logic has several shortcomings. Canary logic is an improvement over the Razor logic. Analogous to the canary bird used by the miners to test a mine, the canary flop can be used to test for possible timing violations.

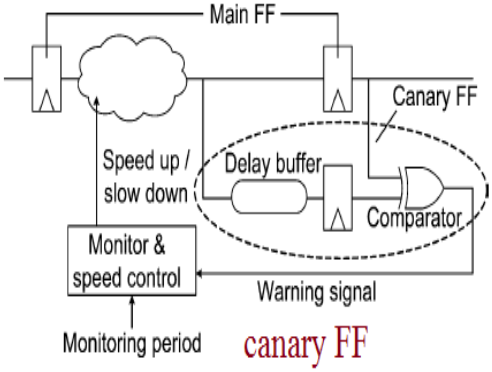

Figure: canary system

The timing error is predicted by comparing the value of the main flop with that of the canary flop. It is obvious from the design mentioned in figure, that data input to the canary flop is delayed instead of clock. So the canary flop will run into timing violation before the main flop .An alert signal triggers a warning for possible timing violations

This design has following advantages over the Razor design:

1. Elimination of delayed clock: The usage of a single phase clock greatly simplifies the design. It also eliminates the short path problem that we counter in the razor flop.
2. Robustness for variations: the delay buffer used in the canary flop has a positive delay. Canary flop will always run into timing error much before the main flop no matter how the PVT variations affect the delay buffer.
3. Protection against timing errors: Canary flop protects the main flop from timing errors i.e. it gives a precautionary warning for timing violations thus preventing timing violations on the main flop, making the correction mechanism redundant. Alert signal here triggers voltage or frequency control.

ALU is taken as a basic digital circuit that is to be connected to canary circuit to observe the output.ALU is connected to canary circuit through CLK.

Arithmetic and Logical Unit:

An arithmetic logic unit (ALU) is a combinational digital electronic circuit that performs arithmetic and bitwise operations on integer binary num
bers.

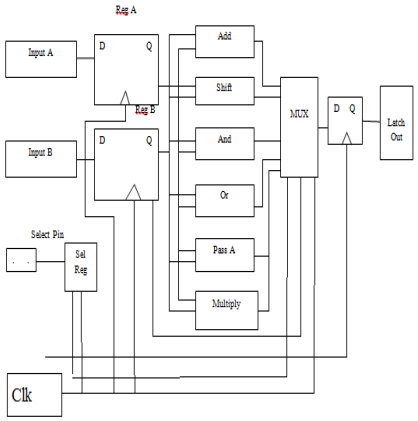

Figure: ALU

Timing Error Detection (TED):

The TED methodology is based on having the system operate at a voltage and frequency point in which the timing of critical paths fails intermittently. These failed timing occurrences are detected and

handled. Whether the target is power or energy savings, the detection and handling overhead has to be lower than the power savings resulting from the lower VDD. When targeting yield, the key is to minimize average overhead (and thereby minimize the overhead power) while ensuring the correct operation for maximal amount of dies at a certain voltage/frequency point.

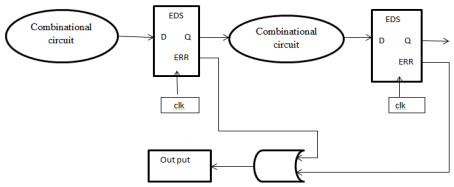

Figure: Block diagram of TED

Timing Error Prevention (TEP):

In our system, we combine TED with time borrowing (TB). When system is timed for zero TB at normal operation, fractionally late signals can be tolerated without errors occurring in the system. However, TB sets timing requirements on the stage subsequent from the stage, namely, the cumulative delay of the two stages cannot exceed the TB window, and therefore TB requires careful design time planning. Combining TED with TB into TEP conceives a system that can tolerate late coming signals, but which does not require special arrangements with regard to stage lengths.

Simplified Power Management for Adaptive Logic:

To maintain high efficiency and ensure a fixed operating voltage, two methods are typically used: 1) multiple topologies to support a changing VBatt tight closed-loop regulation at the output. Both of these previous methods require increasingly complex control circuitry. For dc–dc converters in ultralow-power (ULP) applications, the impact of the control circuitry on efficiency is of particular concern. Therefore, it is difficult to maintain high average efficiency for large changes in VBatt.

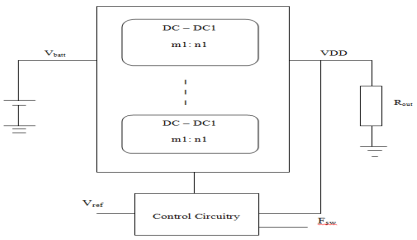

Figure: SC DC-DC converter

In order to maintain high efficiency over a large range of VBatt, the Vref can be linearly adjusted with VBatt. This allows VDD to linearly scale with changes in VBatt. This provides a nearly constant VDD/VBatt ratio. This ratio is called the voltage conversion ratio (VCR) of the dc–dc converter. The ideal VCR, which is n/m, assumes no losses in the converter. The maximum conversion efficiency can be defined in terms of VCR and iVCR

$$\eta max = \frac{VCR}{iVCR} = \left(\frac{m}{n}\right) * \left(\frac{Vdd}{Vbatt}\right) \text{---------2}$$

Allowing for a nearly constant VDD/VBatt for changing VBatt enables ηmax to be achieved for a wide VBatt range. In this paper the scaled input regulation (SIR) technique is defined. The SIR technique requires that the load be able to operate at varying VDD. This requirement is fulfilled with adaptive logic such as TED and TEP. Furthermore, the increasingly flat MEP region of adaptable digital loads translates into an increasingly large operating VDD range with only a minimal penalty for operating outside the MEP. Thus, there is strong motivation to apply the SIR technique to an adaptable digital load that targets the MEP. And if the VDD was allowed to scale with VBatt, then the average conversion rate that could be achieved would be much closer to the peak conversion rate. Again, this requires a load that is able to operate over a large VOUT range without energy loss, for example, a TED system. To rephrase, with adaptable systems, gains might be achieved using voltage conversion instead of voltage regulation.

System simulation

For conventional synchronous systems operating at nominal voltages, a popular solution for overcoming margining has been to use canary circuit is implemented. To work more effectively than previous method basic canary circuit is modified to obtain better results.

Adaptive Load and Dickson Converter System:

The simulated system shown in Fig consists of a 3:1 Dickson dc–dc converter with an adaptive TEP loadin 28-nm FDSOI. The TEP load includes a dual-phase latch pipeline with five stages, time borrow detection circuitry, and adaptive clock generator.

The dc–dc converter used in the simulation is a Dickson 3:1 SC converter. It is a two-phase circuit built with only thin-oxide transistors. The Dickson SC converter has been shown to provide high efficiency across a large load range. The SC dc–dc subtractor circuit provides a reference voltage, which is dependent on VBatt, for the control circuitry. This allows the dc–dc converter to operate over a large range of VBatt using only thin-oxide transistors.

The EDS consists of a pulse generator (I 1, I 2, and XOR1) and a keeper (I5, P2, N3, and N4). A combination of XNOR gate and flip-flop around each stage is added for the verification of correct operation. This verification circuitry is added only to aid the simulation, and would be omitted from a real TEP system.

An active-high stage 1 borrows time from the following active-low stage 2 in the beginning of clock phase n. The lengths of stages 1–3 are exactly one phase under nominal conditions, but due to, e.g., a voltage drop, the propagation time is increased by 25%. Thus, output from stage 2 will be late again and more time is borrowed in the beginning of clock phase n + 1. In such a system, it is possible that consecutive stages each borrow time if the clock period is not sufficiently long. As mentioned, to avoid potential build-up of TB leading to unrecoverable timing violations, the borrowed time must be recovered

Recovery is implemented by a clock control circuit, which is able to stretch the system clock signal (CLK_SYS) by one period. This is achieved by first combining TB event signals (TBE_NEG[n] and TBE_POS[n] in Fig from EDS ports with respective OR trees. The clock control circuit latches the aggregated signal at the beginning of the next phase and excludes a single phase out from the external clock (CLK_EXT) in the case of flagged TB event. To avoid glitches, the gating of CLK_EXT is initiated at the middle of the phase using a 90° shifted reference clock (CLK_REF).

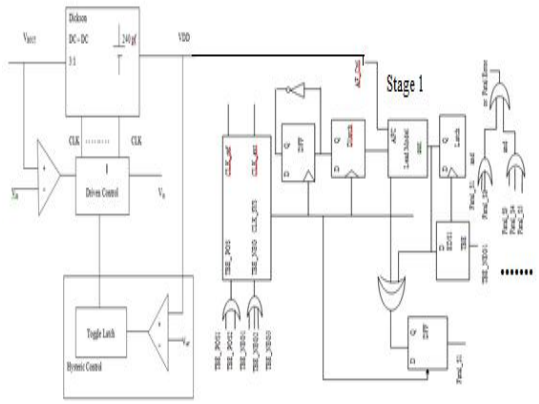

Figure: Adaptive logic circuit

The output of the EDS circuit can become Meta stable in the pulse from the XOR-gate transitions to low at the same time when the keeper is activated, i.e., when the respective latch opens. However, it is unlikely that the signal remain meta stable when it reaches the clock stretching circuitry due to the following reasons.

1) EDS output can become meta stable only at the beginning of the latch transparent phase, and thus, it has a large settling time (1 phase minus OR tree and lock network delay) before captured into the first flip-flop in the clock control circuit.
2) All other EDS outputs would need to be either 0 or meta stable for the OR-tree output to become meta stable.
3) There is slack of almost half a clock phase inside the clock control circuit before the captured input signal is latched using CLK_REF.

The inputs to an ALU are the data to be operated on, called operands, and a code indicating the operation to be performed and, optionally, status information from a previous operation; the ALU's output is the result of the performed operation. In many designs, the ALU also exchanges additional information with a status register, which relates to the result of the current or previous operations.

RESULTS

The following figure shows the simulation result of D flip flop

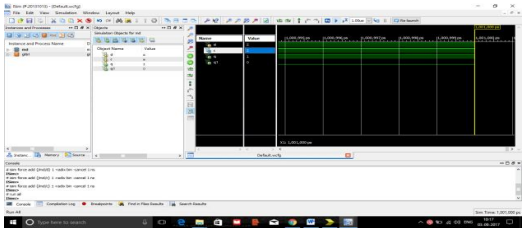

Figure: Simulation results of D flip flop

The following Figure shows simulation result of D latch

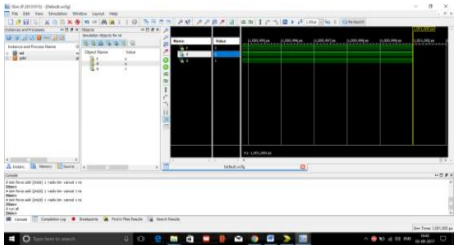

Figure: simulation result of D latch

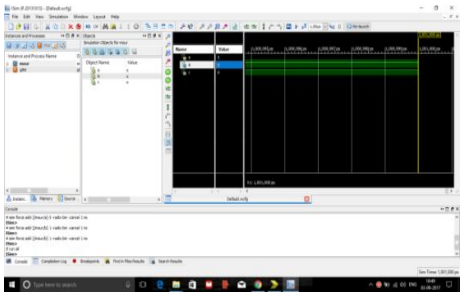

Figure: simulation result of EX-OR Gate

The following Figure shows simulation result of 16-bit ALU connected to adaptive circuit.

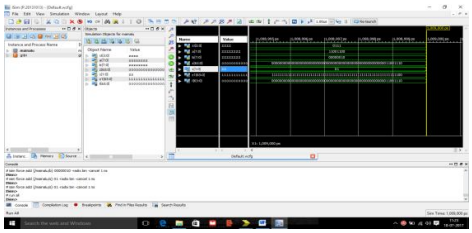

Figure: simulation result of 16-bit ALU

ALU connected to canary circuit:

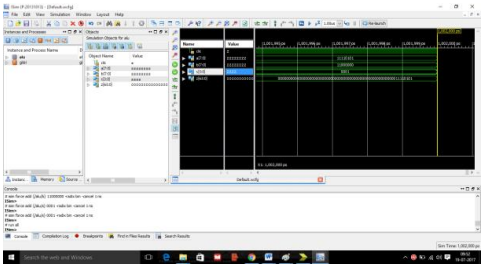

Figure: simulation result of 16-bit ALU connected to canary circuit

ALU connected to adaptive circuit:

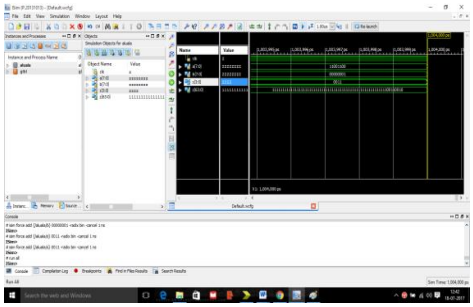

Figure : simulation result of 16-bit ALU connected to Adaptive circuit

Comparison of delay:

Structure	Delay
16-bit ALU	4.776 ns
16-bit ALU connected to canary circuit	3.44 ns
16-bit ALU connected to adaptive circuit	2.414 ns

Table: Comparison of delay

The delay of the proposed method is decreased with compare to others. So the proposed method attained speed in the circuit. The total delay is 2.414 ns, in this time 33.0 % is used for logic and 67.0 % is used for route.

RTL Schematic View:

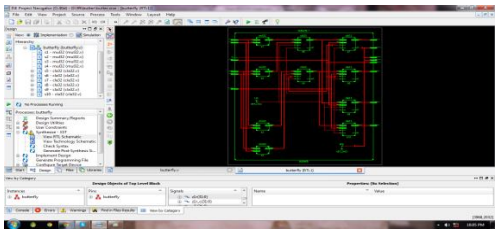

Figure: RTL Schematic View of Adaptive circuit

Observations:

It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx device.

Technology View:

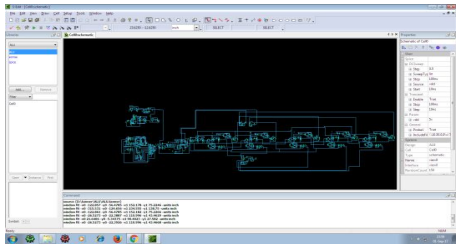

Figure: Technology Schematic View of Adaptive circuit

CONCLUSION

- Delay is generally caused due to errors, to reduce those errors canary circuit is designed to reduce the errors in single shot without the usage of stages. But by using dual latch phase to the circuit the performance of the circuit is improved than the previous method.
- By using dual latch phase, canary circuit and a combination of X-OR gate with flip flop around every stage is added for verification of correction operation results in improved output than the previous method.
- By using adaptive circuit the delay is reduce by 30% compared to the traditional design.

Future Scope of Work:

In this work we decrease the delay of the digital circuit by using adaptive logic. In future delay, area and power of the digital circuit may decrease with further methods.

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