ANALYSIS AND DESIGN OF DOUBLE TAIL COMPARATOR USING A LOW POWER GATING TECHNIQUES

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Abstract: High speed devices such as ADC, operational amplifier are of great importance and for this high speed application a major thrust is given towards low power methodologies. Reduction of power consumption in this device can be achieved by moving towards smaller feature size processes. Comparator is one of the fundamental building blocks in most analog to digital converters. Many high speed analog to digital converters such as flash analog to digital converter require high speed and low power comparators. A new double tail comparator is designed, where the circuit of a conventional double tail comparator is modified for low power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors the positive feedback during the regeneration is strengthened which results in remarkably reduced delay time. Post layout simulation results in a 0.18µm technology confirm the analysis results. It is shown that in the switching transistors using dynamic comparator, both the power consumption and delay time are significantly reduced. Power consumption of conventional double tail comparator is 12µW in 0.8v and power is reduced to 9.5µW in double tail comparator using switching transistors with the same supply voltage.

Keywords—Double tail comparator, dynamic clocked comparator, high speed analog to digital converters, low power analog design, switching transistor, preamplifier based comparators.

I. Introduction

Comparator is a fundamental building block in analog-to-digital converter (ADCs). In design of ADCs, comparator of high speed, low power consumption is used. Comparator in ultra deep sub micrometer (UDSM) technologies suffers from low supply voltage. Hence design of high speed comparator is a challenge when the supply voltage is low. The voltages that appear at the inputs are compared by the comparator that produces a binary output which represents a difference between them. They are critical components in analog-to-digital converters. Designing high-speed comparators becomes more challenging when working with smaller supply voltages. In other words, for a given technology, to attain high speed, transistors with increased width and length values are required to compensate for the reduction of supply voltage, which also means increased chip area and power. So, Transistor width and length are adjusted accordingly for minimum power consumption and maximum operating speed. Hysteresis in the comparator circuit is applied by feeding back a small portion of the output voltage to the positive input.

This feedback voltage adds a polarity-sensitive offset to the input, which results in increased threshold range. A small amount of hysteresis applied to the comparator circuit can prove to be very useful as it reduces the circuit's sensitivity to noise, and also helps reduce multiple transitions occurring at the output if the input is slowly changing its state.

A model for the comparator is developed and discussed, and its functionality is verified by showing a comparison of result

obtained for the proposed model and the existing model. The platform used to develop and analyze the existing model is tanner eda tool.

The research paper is organized as follows: an introduction to CMOS comparator is given, followed by detailed analysis of high speed comparator architecture with properties for each structure will be discussed. Finally, simulation result for all the architecture will be shown and discussed.

II. Material and Methodology

A clocked comparator is a circuit element that makes decision as to whether the input signal is high or low at every clock cycle. Clocked regenerative comparators make fast decision due to strong positive feedback in the regenerative latch. Here analyse the delay of single tail comparator, double tail comparator and proposed comparator.

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1.The operation of the comparator is as follows. During the reset phase when CLK=0andMtail is off, reset transistors (M7–M8) pull both output nodes Outnand Outpto VDDto define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK=VDD, transistors M7 andM8 are off, and Mtail is on. Output voltages (Outp, Outn), which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case whereVINP >VINN, Outp discharges faster than Outn, hence when Outp (discharged by transistor M2 drain current), falls down to VDD–|Vthp | before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor (M5) will turn on initiating the latch regeneration caused by back-to-back inverters (M3, M5 and M4, M6). Thus, Outn pulls to VDD and Outp discharges to ground. If VINP <VINN, the circuits works vice versa. As shown in Fig. 2, the delay of this comparator is comprised of two time delays, t0andtlatch. The delay t0represents the capacitive discharge of the load capacitance CL until the first p-channel transistor (M5/M6) turns on. In case, the voltage at node INP is bigger than INN (i.e.,VINP >VINN), the drain current of transistor M2 (I2) causes faster discharge of Outpnode compared to the Outnnode, which is driven by M1 with smaller current. Consequently, the discharge delay (t0) is given by

$$t_0 = \frac{C_L |V_{thp}|}{I_2} \cong 2\frac{C_L |V_{thp}|}{I_{tail}}. \qquad (1)$$

In (1), since I2=Itail/2+ ∆ Iin =Itail/2+gm1,2 Vin,for small differential input (Vin), I2 can be approximated to be constant and equal to the half of the tail current. The second term,t latch, is the latching delay of two cross coupled inverters. It is assumed that a voltage swing of Vout =VDD/2 has to be obtained from an initial output voltage differenceV0 at the falling output (e.g., Outp). Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch. Hence, the latch delay time is given by,

$$t_{latch} = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right)$$

Where gm,eff is the effective transconductance of the back-to back inverters. In fact, this delay depends, in a logarithmic manner, on the initial output voltage difference at the beginning of the regeneration (i.e., at t =t0). Based on (1), V0 can be calculated from (3)

$$\Delta V_0 = \left|V_{outp}(t = t_0) - V_{outn}(t = t_0)\right|$$
$$= \left|V_{thp}\right| - \frac{I_2 t_0}{C_L} = \left|V_{thp}\right|\left(1 - \frac{I_2}{I_1}\right).$$

The current difference, Iin =|I1Δ−I2|, between the branches is much smaller than I1 and I2. Thus, I1 can be approximated by Itail/2 and (3) can be rewritten as

$$\begin{aligned}\Delta V_0 &= \left|V_{thp}\right| \frac{\Delta I_{in}}{I_1} \\ &\approx 2\left|V_{thp}\right| \frac{\Delta I_{in}}{I_{tail}} \\ &= 2\left|V_{thp}\right| \frac{\sqrt{\beta_{1,2} I_{tail}}}{I_{tail}} \Delta V_{in} \\ &= 2\left|V_{thp}\right| \sqrt{\frac{\beta_{1,2}}{I_{tail}}} \Delta V_{in}.\end{aligned}$$

In this equation, β1, 2 is the input transistors' current factor and Itail is a function of input common-mode voltage (Vcm) and VDD. Now, substituting V0in latch delay expression and consideringt0, the expression for the delay of the conventional dynamic comparator is obtained as Equation (5) explains the impact of various parameters.

$$\begin{aligned}t_{delay} &= t_0 + t_{latch} \\ &= 2\frac{C_L\left|V_{thp}\right|}{I_{tail}} + \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}}{4\left|V_{thp}\right| \Delta V_{in}} \sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right).\end{aligned}$$

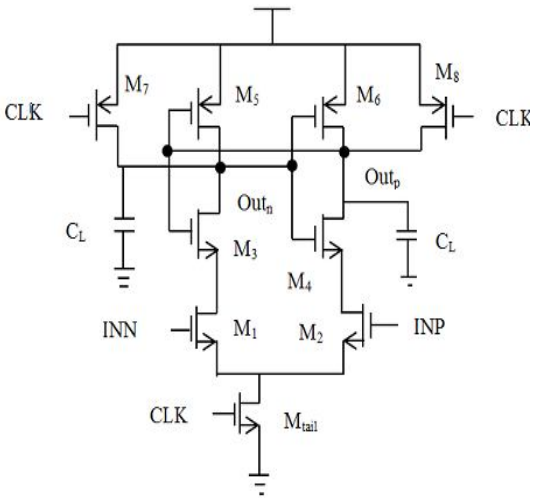
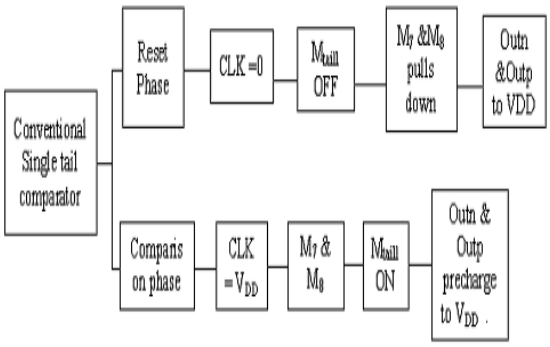


Fig: 1.1 Schematic diagram of conventional single tail comparator



The total delay is directly proportional to the comparator load capacitance CL and inversely proportional to the input difference voltage (Vin). Besides, the delay depends indirectly to the input common-mode voltage (Vcm). By reducing Vcm, the delay t0of the first sensing phase increases because lower Vcm causes smaller bias current (Itail).On the other hand, (4) shows that a delayed discharge with smaller Itail results in an increased initial voltage difference (V0), reducing tlatch. Simulation results show that the effect of reducing the Vcm on increasing of t0 and reducing off latch will finally lead to an increase in the total delay. it has been shown that an input common-mode voltage of 70% of the supply voltage is optimal regarding speed and yield.

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistorsM3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5orM6to start complete regeneration. At a low supply

voltage, this voltage drop only contributes a small gate-source voltage for transistorsM3andM4, where the gate source voltage ofM5andM6is also small; thus, the delay time of the latch becomes large due to lower transconductance.

Another important drawback of this structure is that there is only one current path, via tail transistor M tail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a. large tail current would be desirable to enable fast regeneration in the latch. Besides, as far as Mtail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

B. Conventional Double-Tail Dynamic Comparator

A conventional double-tail comparator is shown in Fig. 3. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and widerMtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset.

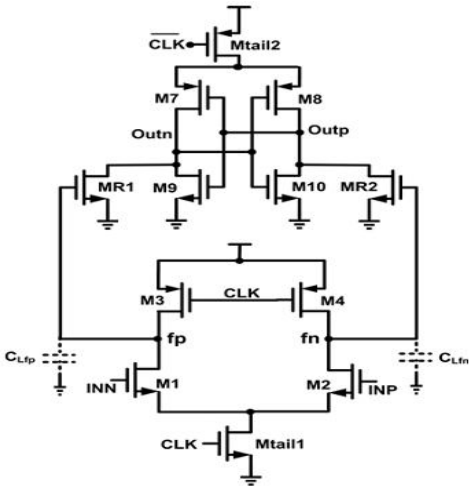
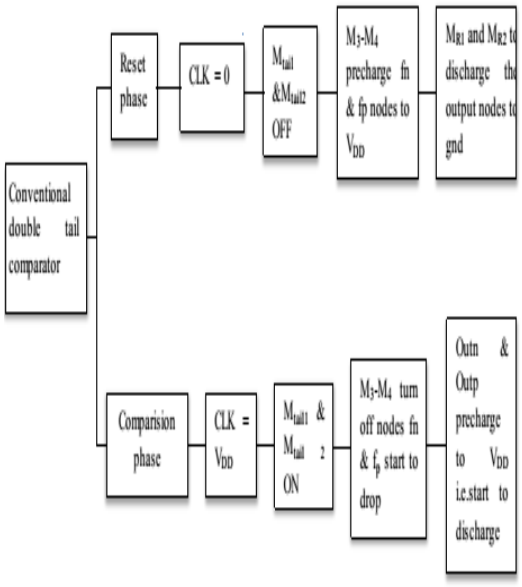


Fig. 3. Schematic diagram of the conventional double-tail dynamic comparator



The operation of this comparator is as follows (see Fig. 4). During reset phase (CLK=0, Mtail1,and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1andMR2to discharge the output nodes to ground. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and on top of this, an input-dependent differential voltage Vfn(p) will build up. The intermediate stage formed by MR1and MR2passes Vfn(p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise.

Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts,t0 and tlatch . The delayt0 represents the capacitive charging of the load capacitance Clout (at the latch stage output nodes, Outnand Outp) until the first n-channel transistor (M9/M10) turns on, after which the latch regeneration starts; thust0 is obtained from

$$t_0 = \frac{V_{Thn} C_{Lout}}{I_{B1}} \approx 2\frac{V_{Thn} C_{Lout}}{I_{tail2}}$$

From the equations derived for the delay of the double-tail dynamic comparator, some important notes can be concluded.

1) The voltage difference at the first stage outputs (Vfn/fp) at timet0has a profound effect on latch initial differential output voltage (V0) and consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparator.

2) In this comparator, both intermediate stage transistors will be finally cut-off, (since fn and fp nodes both discharge to the ground), hence they do not play any role in improving the effective transconductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to VDD, which means power consumption. The following section describes how the proposed comparator improves the performance of the double-tail comparator from the above points of view.

III. Proposed Double-Tail Dynamic Comparator

As long as fn continuously falling, the corresponding PMOS control transistors (Mc1 in this case) starts to turn on, pulling fp nodes back to the VDD; so another control transistors (Mc2) remains off, allowing fn to be discharged completely. In other words unlike conventional double tail dynamic comparators which in Vfn/fp is just a functions of input transistors transconductance of input voltage difference in the proposed structures as soon as the comparator detects for the instance nodes fn discharging faster, a PMOS transistors (Mc1) turns on, pulling the other nodes fp back to the VDD.

Fig. 5 demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase Vfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner [see Fig**.** 5(a)].

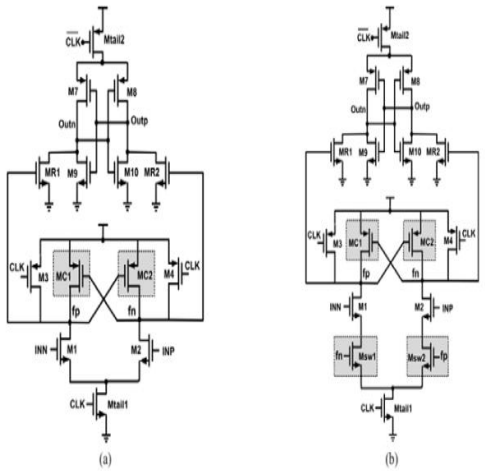


Fig. 5. Schematic diagram of the proposed dynamic comparator. (a) Main idea. (b) Final structure

A. Operation of the Proposed Comparator

The operation of the proposed comparator is as follows (see Fig. 6). During reset phase (CLK=0, Mtail1 andMtail2 are off, avoiding static power),M3andM4pulls both fn and fp nodes to VDD, hence transistor Mc1andMc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision-making phase (CLK=VDD, Mtail1,and Mtail2 are on), transistorsM3andM4turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose VINP >VINN, thus fn drops faster than fp, (since M2provides more current thanM1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which Vfn/fp is just a function of input transistor transconductance and input voltage difference (9), in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (Mc1) turns on, pulling the other node

fp back to the VDD. Therefore by the time passing, the difference between fn and fp (Vfn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time . Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g.,Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, andMtail1), resulting in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors [Msw1 andMsw2,as shown in Fig. 5(b)].

At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to VDD (during the reset phase), both switches are closed and fn and fp tart to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the VDD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn fromVDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch. This will be more discussed in the following section.

B. Delay Analysis

In order to theoretically demonstrate how the delay is reduced, delay equations are derived for this structure as previously done for the conventional dynamic comparator and the conventional double-tail dynamic comparator. The analysis is similar to the conventional double-tail dynamic comparator, however; the proposed dynamic comparator enhances the speed of the double-tail comparator by affecting two important factors: first, it increases the initial output voltage difference V0) at the beginning of the regeneration (t =t0); and second, it enhances the effective transconductance (gmeff) of the latch. Each of these factors will be discussed in detail.

1) Effect of Enhancing V0:

As discussed before, we define t0, as a time after which latch regeneration starts. In other words,t0is considered to be the time it takes (while both latch outputs are rising with different rates) until the first nMOS transistor of the back-to-back inverters turns on, so that it will pull down one of the outputs and regeneration will commence. According to (2), the latch output voltage difference at time t0,(V0) has a considerable impact on the latch regeneration time, such that bigger V0 results in less regeneration time. Similar to the equation derived for the V0of the double-tail structure, in this comparator we have

$$\begin{aligned}\Delta V_0 &= V_{\mathrm{Thn}}\frac{\Delta I_{\mathrm{latch}}}{I_{\mathrm{B1}}}\\ &\approx 2V_{\mathrm{Thn}}\frac{\Delta I_{\mathrm{latch}}}{I_{\mathrm{tail2}}}\\ &= 2V_{\mathrm{Thn}}\frac{g_{\mathrm{mR1,2}}}{I_{\mathrm{tail2}}}\Delta V_{\mathrm{fn/fp}}.\end{aligned}$$

In order to find Vfn/fp at t =t0, we shall notice that the combination of the control transistors (Mc1 andMc2) with two serial switches (Msw1, Msw2) emulates the operation of a back to-back inverter pair; thus using small-signal model presented, Vfn/fp is calculated by

$$\Delta V_{\mathrm{fn/fp}} = \Delta V_{\mathrm{fn(p)0}}\exp((A_{\mathrm{v}}-1)t/\tau).$$

2) Effect of Enhancing Latch Effective Transconductance:

As mentioned before, in conventional double-tail comparator, both fn and fp nodes will be finally discharged completely. In our proposed comparator, however, the fact that one of the first stage output nodes (fn/fp) will charge up back to the VDD at the beginning of the decision making phase, will turn on one of the intermediate stage transistors, thus the effective transconductance of the latch is increased. In other words, positive feedback is strengthened.

By comparing the expressions derived for the delay of the three mentioned structures, it can be seen that the proposed comparator takes

advantage of an inner positive feedback in double-tail operation, which strengthen the whole latch regeneration. This speed improvement is even more obvious in lower supply voltages. This is due to the fact that for larger values of VTh/VDD, the transconductance of the transistors decreases, thus the existence of an inner positive feedback in the architecture of the first stage will lead to the improved performance of the comparator. Simulation results confirm this matter.

$$t_{latch} = \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} \cdot \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right). \quad (16)$$

Finally, by including both effects, the total delay of the proposed comparator is achieved from

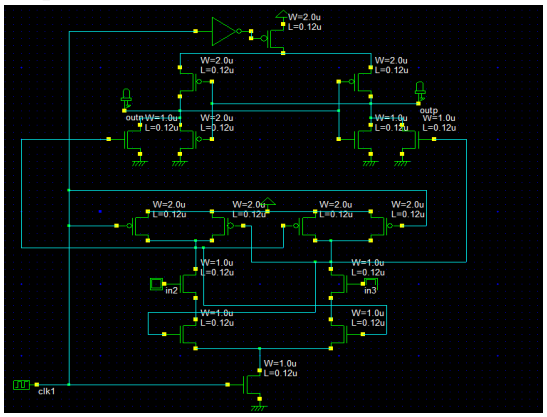
$$t_{delay} = t_0 + t_{latch} = 2\frac{V_{Thn} C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff} + g_{mr1,2}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) = 2\frac{V_{Thn} C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}} \times \ln\left(\frac{V_{DD}/2}{4V_{Thn}\left|V_{Thp}\right| \frac{g_{mR1,2}}{I_{tail2}} \frac{g_{m1,2}\Delta V_{in}}{I_{tail1}} \exp\left(\frac{G_{m,eff1} \cdot t_0}{C_{L,fn(p)}}\right)}\right). \quad (17)$$

3) Reducing the Energy per Comparison:

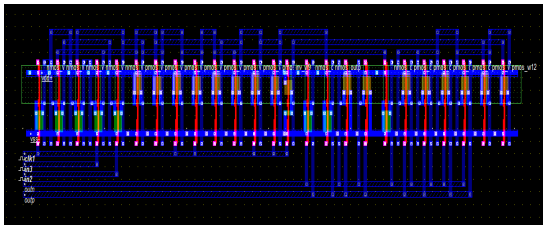
It is not only the delay parameter which is improved in the modified proposed comparator, but the energy per conversion is reduced as well. As discussed earlier, in conventional double-tail topology, both fn and fp nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the VDD. However, in our proposed comparator, only one of the mentioned nodes (fn/fp) has to be charged during the reset phase. This is due to the fact that during the previous decision making phase, based on the status of control transistors, one of the nodes had not been discharged and thus less power is required. This can be seen when being compared with conventional topologies.

IV. Simulation Results

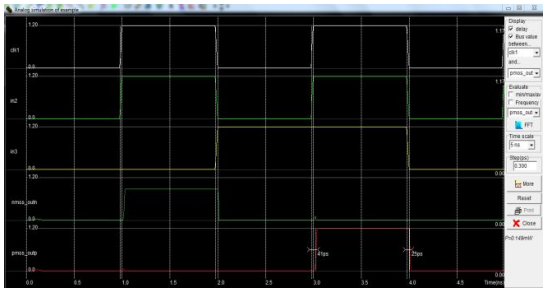
Proposed Schematic.



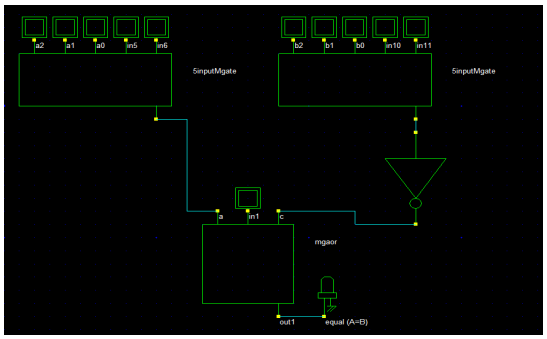
Layout Design.



Simulation.



Extension, Schematic.



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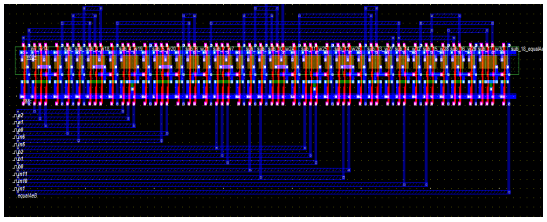
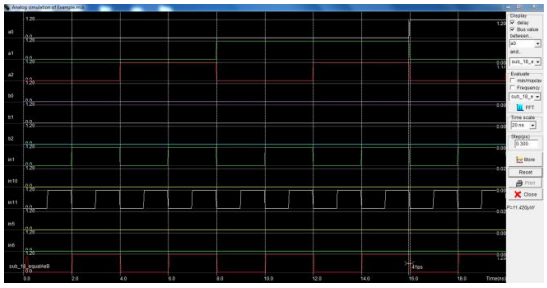


Simulation.



V. Conclusion

In this paper, an analysis for clocked dynamic comparators is presented. One structure of double-tail dynamic comparators was analysed. Also, based on analyses, a new dynamic comparator with low-voltage low power capability was proposed in order to improve the performance of the comparator. Simulation results in 0.18-µm CMOS technology confirmed that the delay and power consumption of the proposed comparator is reduced to a great extent in comparison with the existing double-tail comparator. The proposed comparator can be used for the design of high speed ADCs as the delay is reduced and hence the operation will be faster.

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