CAPACITANCE REDUCTION CONTROL STRATEGY FOR SINGLE PHASE PHOTO VOLTAIC QUASI Z SOURCE INVERTER USING DOUBLE FREQUENCY RIPPLE SUPPRESSION CONTROLLER

[1]GOVINDRAO, [2]MAHAMMAD ANWAR
[1]M.Tech, Ballari institute of Technology and management Engineering College Affiliated to VTU, Belagavi, Karnataka, India.
[2]Assistant Professor, Ballari institute of Technology and management Engineering College Affiliated to VTU, Belagavi, Karnataka, India.

ABSTRACT- In single phase photovoltaic system (PV), there exist a double frequency jumble that exist between the dc input side and air conditioning output side. To cradle out the twofold frequency swell energy it is important to required. A capacitance lessening control technique is proposed to support the DFR energy in single-phase Z-source/semi Z-source inverter applications is proposed in this paper. In single-organize photovoltaic (PV) system, there is a power anomaly exist between the AC output and DC input. The double frequency swell (DFR) energy should be supported by passive network. The swell energy will flow into the info side and unfavorably influence the PV energy harvest. In a conventional PV system, because of their high capacitance electrolytic capacitors are typically utilized. Electrolytic capacitors are thought to be a standout amongst the most disappointment inclined components in a PV inverter. The proposed control procedure can fundamentally lessen the capacitance necessity and accomplish low input voltage DFR. Therefore, exceedingly solid film capacitors can be utilized. Due to the proposed control system the expanded switching device voltage stress and power loss will likewise be examined. By utilizing the simulation results we can investigate the proposed strategy.

Index Terms—Capacitance reduction, double-frequency ripple (DFR), Z-source (ZS)/quasi-Z-source (qZS).

I.INTRODUCTION

In the recent years for the photovoltaic application the voltage fed z-source inverter and quasi z-source inverters are considered. This inverter feature single stage buck - boost transformer. It is due to shoot through capability. For the single phase and three phase applications the z-source inverter and quasi z source inverter are utilized. The voltage-fed z-source inverter (ZSI) and quasi-Z-source inverter (qZSI) has been considered for photovoltaic (PV) application in recent years [1-3]. These inverters feature single-stage buck-boost and improved reliability due to the shoot-through capability. The ZSI and qZSI are both utilized in three-phase and single-phase applications [1-5]. The single phase ZSI/qZSI can also be connected in cascaded structure for higher voltage application and higher performance.

The mismatched ac ripple is termed as double-frequency ripple (DFR) in this paper. In three-phase applications, the Z-source (ZS)/ quasi-Z-source (qZS) network only needs to be designed to handle the high frequency ripples. However, in single-phase application, the ZS/qZS network needs to handle not only the high-frequency ripples but also the low-frequency ripple. The qZSI will be used in this paper to study the low-frequency ripple issue and present the proposed control strategy. A single-phase qZSI system is shown in Fig. 1.

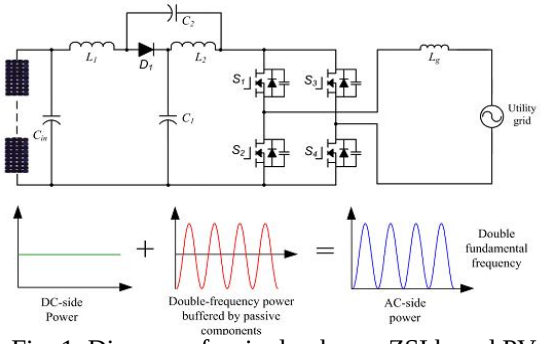


Fig. 1. Diagram of a single-phase qZSI based PV system.

Ideally, the dc-side output power is pure dc and the ac-side power contains a dc component plus ac ripple component whose frequency is two times the grid voltage frequency. The mismatched ac ripple is termed as double-frequency ripple (DFR) in this paper. In order to study the low frequency ripple issues qZSI is used in this paper. A single phase qZSI system is shown in fig.1. The output power at DC side is pure DC and AC side power contains DC component plus AC ripple component whose frequency is two times the grid frequency. The mismatched AC ripple in the system is coined as double frequency ripple (DFR).

In this paper, a new control strategy is proposed for ZSI/ qZSI to mitigate the input DFR without using large capacitance, which enables us to

use the highly reliable film capacitors. There is no extra hardware needed to implement the capacitance reduction. The proposed control system incorporates a modified modulation strategy and a DFR suppression controller. The gallium nitride (GaN) devices are applied in the inverter to increase the system efficiency at high switching frequency. Finally, experimental results are provided to verify the effectiveness of the proposed control system.

In order to balance the power mismatch between the dc side and ac side, the DFR power needs to be buffered by the passive components, mainly the qZS capacitor C1 which has higher voltage rating than C2. The DFR peak power is the same as the dc input power, so large capacitance is needed to buffer this ripple energy. To achieve high inverter power density with reasonable cost, electrolytic capacitors are usually selected. Electrolytic capacitors contain a complex liquid chemical called electrolyte to achieve high capacitance and low series resistance. As the electrolytic capacitors age, the volume of liquid present decreases due to evaporation and diffusion.

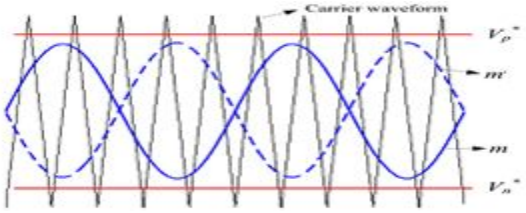
Two additional smoothing-power circuits are employed to reduce the DFR of DC-link voltage in ZSI. However, the added circuits increase the system cost and complexity. A low-frequency harmonic elimination PWM technique is presented to minimize the double frequency ripple on Z-source capacitors. However, the method is used for application with constant voltage input source and double-frequency ripple current is induced in the inductor and the input side. This is not suitable for the PV application, because the ripple current will decrease the energy harvest from the PV panels.

II.PROPOSED CONTROL SYSTEM FOR CAPACITANCE REDUCATION

The basic principle of the proposed capacitance reduction method can be explained by (1).

$$\Delta E = \frac{1}{2}C(v_{C-max}^2 - v_{C-min}^2) \quad (1)$$

where C is the capacitance, ΔE is the ripple energy that is stored in the capacitor, and vC-max and vC-min are the maximum and minimum voltages across the capacitor. According to (1), there are two ways to increase ΔE. One is to increase the capacitance C, and the other way is to increase the voltage fluctuation across the capacitor. Instead of increasing the capacitance, the proposed control system will increase the voltage fluctuation across the qZS capacitors to buffer more double-frequency power. A dedicated strategy is needed to impose the DFR on qZS capacitors while preventing the ripple energy from flowing into the input. In order to achieve this, a modified modulation strategy and an input DFR suppression controller are presented.

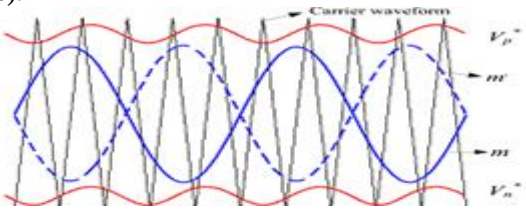


(a)

Fig. 2. The modulation strategy of (a) traditional method

In conventional single-phase qZSI, the modulation strategy is shown in Fig. 2(a). The two phase legs of the full bridge are modulated with 180o opposed reference waveforms, m and , m , to generate three-level voltage output. Two straight lines v_p^* and v_n^* are used to generate the shoot through duty ratio. When the triangular carrier is greater than v*p or the carrier is smaller than * vn , all four switches S1 − S4 turn on simultaneously for shoot-through.

In the proposed control system, the shoot-through control lines v_p^* and v_n^* are modified to a line with doublefrequency component as shown in Fig. 2(b).



(b)

Fig. 2. The modulation strategy of (b) proposed method.

By doing so, the dc side and the qZS capacitor DFR can be decoupled. An input DFR suppression controller is added in the control system to generate the double-frequency component in v_p^* and v_n^*

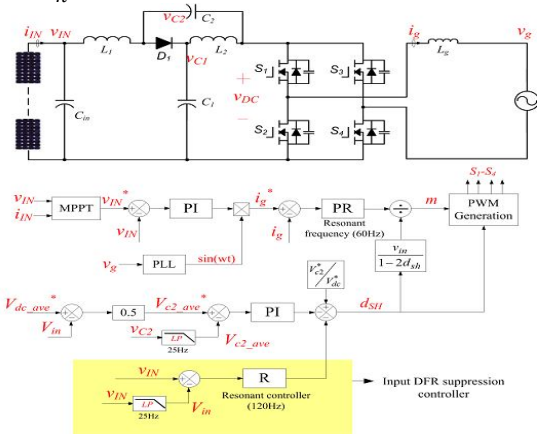


Fig. 3. Diagram of the proposed control system.

Fig. 3 shows the detailed control system diagram of the proposed single-phase qZSI. The proposed control contains the maximum power point tracking (MPPT) controller, grid connected current controller, qZS capacitor voltage controller and input DFR suppression controller. The MPPT controller provides the input voltage reference v_{IN}^*. The error between v_{IN}^* and v_{IN} is regulated by a PI controller and its output is the magnitude of the grid current reference. The grid current i_g is regulated by controlling the inverter modulation index m through a proportional resonant (PR) controller. The PR controller has a resonance frequency equal to the grid frequency. The qZS capacitor voltage is regulated by controlling d_{SH}. If the inverter loss is not enough to damp the oscillation, dedicated active damping is needed to deal with the oscillation and vC2 information is required for the implementation. Due to the limited space, the detail of the active damping is not presented in this paper and will be covered in future paper. The vC2 voltage controller only regulates the average value of vC2, which is Vc2_ave, due to the low-pass filter in the signal feedback with a cutoff frequency of 25Hz. Therefore, the capacitor voltage controller has limited influence on double frequency component and most DFR energy can be kept in qZS capacitors. Vdc_ave* should be selected carefully so that the value of dSH does not become negative because of the double-frequency swing, and the summation of dSH and m is always smaller than 1. A feed forward component Vc2*/ $V_{dc\_ave}^*$ is added to the output of the capacitor voltage controller to increase the dynamic performance.

III.IMPACT OF CAPACTICANCE REDUCTION

A. System stability

In order to apply the proposed control system, it is necessary to study impact of decreasing C1 on system stability. The possible operation states of voltage fed qZSI have been presented in and it is summarized in the appendix with equivalent circuits, and the averaged model of qZSI can be obtained as in (2).

$$\begin{cases} L_1\frac{di_{L1}}{dt} = \left(1+\frac{T_{AB}+T_{0B}}{T_s-T_{AB}-T_{0B}}\right)(v_{C1}+v_{C2})d_{SH} + \frac{T_{SBU}}{T_s-T_{AB}-T_{0B}}(v_{C1}+v_{C2}) - v_{C1} + v_{1N} \\ L_2\frac{di_{L2}}{dt} = \left(1+\frac{T_{AB}+T_{0B}}{T_s-T_{AB}-T_{0B}}\right)(v_{C1}+v_{C2})d_{SH} + \frac{T_{SBU}}{T_s-T_{AB}-T_{0B}}(v_{C1}+v_{C2}) - v_{C2} \\ C_1\frac{dv_{C1}}{dt} = i_{L1} - (i_{L1}+i_{L2})d_{SH} - \frac{T_{SBU}}{T_s}(i_{L1}+i_{L2}) - \left(\frac{T_{AC}}{T_s}+\frac{T_{AB}}{T_s}\right)i_{DC} \\ C_2\frac{dv_{C2}}{dt} = i_{L2} - (i_{L1}+i_{L2})d_{SH} - \frac{T_{SBU}}{T_s}(i_{L1}+i_{L2}) - \left(\frac{T_{AC}}{T_s}+\frac{T_{AB}}{T_s}\right)i_{DC} \end{cases} \quad (2)$$

where T s is the switching period, TAB, T0B, TSBU, TAC, and TSBI are time intervals of different operation states, as listed in the appendix, m is the modulation signal and dSH = TSBI / Ts. The small signal model can be derived accordingly as in (3).

$$\begin{cases} L_1\frac{d\hat{\imath}_{L1}}{dt} = \left(1+\frac{T_{AB}+T_{0B}}{T_s-T_{AB}-T_{0B}}\right)(v_{C1}+v_{C2})\hat{d}_{SH} + \frac{T_{SBU}}{T_s-T_{AB}-T_{0B}}(\hat{v}_{C1}+\hat{v}_{C2}) - (1-D_{sh})\hat{v}_{C1} + D_{sh}\hat{v}_{C2} + v_{1N} \\ L_2\frac{di_{L2}}{dt} = \left(1+\frac{T_{AB}+T_{0B}}{T_s-T_{AB}-T_{0B}}\right)(v_{C1}+v_{C2})d_{SH} + \frac{T_{SBU}+T_{AB}+T_{0B}}{T_s-T_{AB}-T_{0B}}(\hat{v}_{C1}+\hat{v}_{C2}) - (1-D_{sh})\hat{v}_{C2} + D_{sh}\hat{v}_{C1} \\ C_1\frac{d\hat{v}_{C1}}{dt} = \left(1-D_{Sh}-\frac{T_{SBU}}{T_s}\right)\hat{\imath}_{L1} - \left(D_{Sh}+\frac{T_{SBU}}{T_s}\right)\hat{\imath}_{L2} + (I_{l1}+I_{l2})\hat{d}_{SH} - \left(\frac{T_{AC}}{T_s}+\frac{T_{AB}}{T_s}\right)\hat{\imath}_{DC} \\ C_1\frac{d\hat{v}_{C1}}{dt} = \left(1-D_{Sh}-\frac{T_{SBU}}{T_s}\right)\hat{\imath}_{L1} - \left(D_{Sh}+\frac{T_{SBU}}{T_s}\right)\hat{\imath}_{L2} + (I_{l1}+I_{l2})\hat{d}_{SH} - \left(\frac{T_{AC}}{T_s}+\frac{T_{AB}}{T_s}\right)\hat{\imath}_{DC} \end{cases} \quad (3)$$

This RHP zero will limit the system dynamic response. However, the decrease of C1 will not significantly change the position of the RHP zero. There are two pairs of conjugated poles located on the imaginary axis, which indicate possible resonances at two different frequencies. The lower-frequency resonance is more related to C1 and the higher-frequency resonance is mainly determined by C2. Therefore, it is seen that the higher resonant frequency does not change much with the C1 change. The lower resonant frequency increases when C1 decreases. Because there is always a zero close to the lower-frequency pole, the lower-frequency resonance is largely damped. Decreasing C1 does not affect the system stability much.

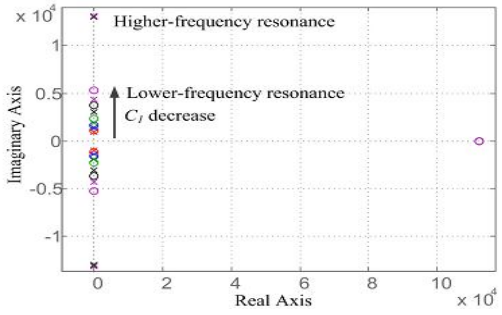


Fig. 4. Root loci of the system with C1 parameter sweeping.

B. Increased device voltage stress and power loss

When the proposed method is applied, the double frequency voltage ripple across vC1 and vC2 will be increased intentionally. The dc link voltage across the H-bridge v_{DC} will also include DFR which could increase the voltage stress of switching devices. Because vC1 is much higher than vC2, most double-frequency energy is stored in C1. The value of vC1 can be calculated using the following equation

$$\frac{1}{2}C_1 v_{C1}^2 = \frac{1}{2}C_1 v_{C1-ave}^2 + \int_0^t (P_{in} - P_{AC})dt \quad (4)$$

Where v_{C1-ave} is the average value of v_{C1}, P_{in} is the input power and P_{AC} is the instantaneous ac output power. P_{AC} can be calculated in (6).

$$PAC = V_{g-p}\sin(\omega t) * I_{g-p}\sin(\omega t) = \frac{1}{2}V_{g-p}I_{g-p}[1 - cos(2\omega t)] = P_{in}[1 - cos(2\omega t)] \quad (5)$$

where V_{g_p} and I_{g_p} are the peak value of vg and ig. Therefore, we can get

$$v_{C1} = v_{C1-ave} + \Delta v_{C1-dfr} = \sqrt{V_{C1-ave}^2 + \frac{Pin}{\omega C_1}\sin(2\omega t)} = \sqrt{\left(\frac{V_{dc-ave}+V_{in}}{2}\right)^2 + \frac{Pin}{\omega C_1}\sin(2\omega t)} \quad (6)$$

where $+\Delta v_{C1-dfr}$ is the DFR component of v_{C1}. In (7), the value of V_{in} and P_{in} are determined by the PV array operating point. V_{dc-ave} is indirectly controlled by regulating V_{C2-ave} as shown in Fig.3. Therefore, when $V_{dc\_ave}^*$ is selected and the PV array operating point is determined, vC1 can be calculated. It is seen that larger v_{C1-dfr} can reduce the size of C1. v_{DC} during non-shoot period can be obtained as

$$v_{DC} = 2v_{C1} - v_{in} = 2\sqrt{\left(\frac{V_{dc-ave}+V_{in}}{2}\right)^2 + \frac{P_{in}}{\omega C_1}\sin(2\omega t)} - V_{in} \quad (7)$$

It is seen from (8), when C1 and Pin are fixed, the switching device voltage stress is mainly determined by V_{dc-ave} and V_{in}. There is an optimized value of $V_{dc\_ave}^*$ for different input voltage conditions to minimize the switching device voltage stress.

$$m = \frac{V_{g-p}\sin(\omega t)}{v_{DC}} \quad (8)$$

In order to take advantage of the buck-boost feature of the qZSI, the input voltage range is usually selected that V_{g-p} is among the input voltage range. For the proposed method, the maximum switching device voltage stress could happen at maximum or minimum V_{in}. When V_{in} is larger than V_{g-p}, no shoot-through is needed in conventional design and dSH equal to zero. However, for the proposed method, certain value of D sh_ave is needed to make sure dSH does not become negative values because of the double-frequency swing. Higher Vin leads to higher peak value of vDC. Therefore, one of the worst cases for the increased device voltage stress could happen at maximum Vin.

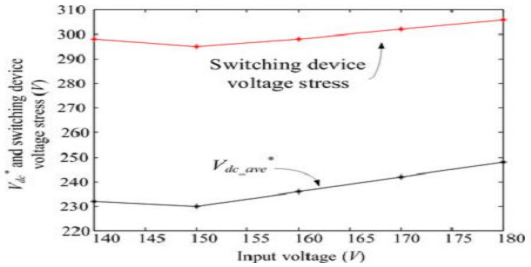


Fig. 5. $V_{dc\_ave}^*$ and switching device voltage stress at different input voltages.

IV.SIMULATION RESULTS

For the proposed method, there is a design trade-off between the demand of decreasing C1 and the increased voltage stress across the switching devices.

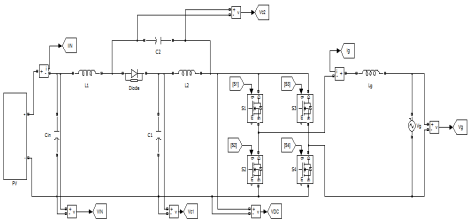


Fig.6 Block diagram of simulation

TABLE I.
PARAMETERS OF THE QZSI UNDER STUDY

qZSI Component	Parameters
Input voltage v_{IN}	140-180V
Grid voltage v_g	120Vrms
C_1	2mF for conventional system 200μF for proposed system
C_2	20μF
L_1	330μH
L_2	215μH
L_g	600μH
Switching frequency	100kHz

They are provided in Fig. 5. It is seen that the maximum voltage stress across the switching devices happens at Vin=180V in this design.

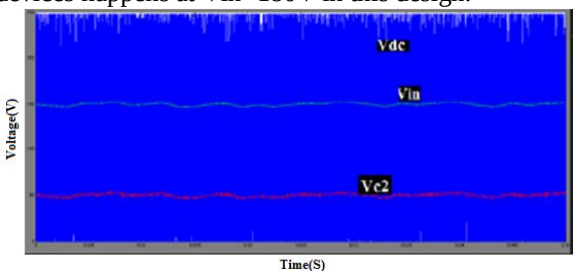


Fig. 7. The v_{DC}, v_{IN} and vC2 waveforms of the qZSI with the conventional control, C1=2mF.

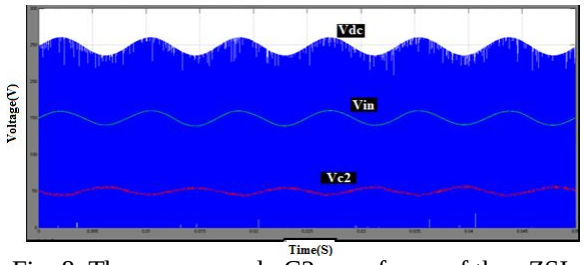


Fig. 8. The v_{DC}, v_{IN} and vC2 waveforms of the qZSI with the conventional control, C1=200µF

The waveforms for the qZSI with 200µF capacitor, but without the proposed control, are provided in Fig. 8. The waveforms of the system with the proposed control strategy are shown in Fig. 9.

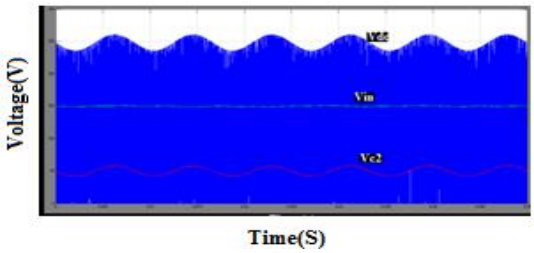


Fig. 9. The v_{DC}, v_{IN} and vC2 waveforms of the qZSI with the proposed control, C1=200µF.

The efficiency comparison of the conventional qZSI and the qZSI with proposed control at different power outputs is provided in Table. II.

TABLE II.
EFFICIENCY COMPARISON OF THE CONVENTIONAL QZSI AND QZSI WITH THE PROPOSED CONTROL

	300W	400W	500W	600W
C_1=2mF with conventional control	93.05%	93.18%	93.66%	93.76%
C_1=200µF with proposed control	92.36%	93.06%	93.48%	93.55%

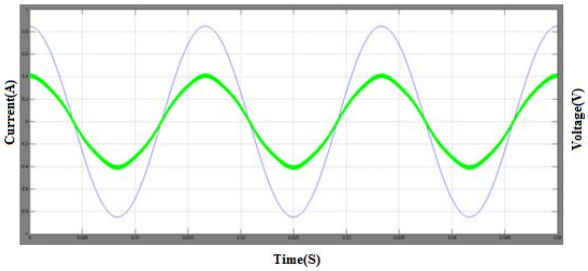


Fig. 10. The output current waveform of the qZSI with the proposed control, C1=200µF.

V.CONCLUSION

A new control strategy is proposed to minimize the capacitance requirement in single-phase qZSI PV system. The proposed control system incorporates a modified modulation strategy and a DFR suppression controller. Instead of using large capacitance, the qZS capacitors are imposed with higher double-frequency voltages to store the double-frequency ripple energy. In order to prevent the ripple energy flowing into the input PV side, a modified modulation and an input DFR suppression controller are used to decouple the input voltage ripple from the qZS capacitor DFR. The small signal model is developed and shows that the capacitance reduction does not impact the system stability. In this paper capacitance reduction control strategy is proposed to buffer the DFR energy in Z source or Quasi Z source inverter application. The proposed control strategy can significantly reduced the capacitance requirement without using any extra hardware component. This can also achieve low input voltage DFR. Consequently a highly reliable film capacitors can used.

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GOVINDRAO

Completed B.E in Electrical & Electronics Engineering in 2014 from VTU Belagavi, KARNATAKA and Pursuing M.Tech from Ballari institute of Technology and management Engineering College Affiliated to VTU, Belagavi, Karnataka, India. Area of interest includes Power Electronics.
E-mail id: govindkulkarni719@gmail.com

MAHAMMAD ANWAR

Completed B.E Electrical & Electronics Engineering in 2007 from S.T.J.I.T College Ranebennur affliated to VTU, KARNATAKA and M.Tech in Power Electronics in 2011 from PDA College Gulbarga, Karnataka. Working as Assistant Professor at BITM Engineering college Ballari, Karnataka India. Area of interest includes Power electronics, Electrical drives control.
E-mail id:anwar017akill017@gmail.com