# INTEGRATION OF SEVEN-LEVEL INVERTER WITH SINGLE DC SOURCE USING SWITCHED-CAPACITOR TECHNIQUES

**VASUDEV**
M.Tech,Ballari institute of Technology and management Engineering College, Belagavi, Karnataka, India.

**ABSTRACT- A novel cascaded seven-level inverter topology with a solitary information source incorporating exchanged capacitor methods is proposed in this paper. The proposed topology replaces all the different dc sources with capacitors, leaving just a single H-bridge cell with a genuine dc voltage source and just includes two accusing switches contrasting of the customary course multilevel inverter. The capacitor charging circuit contains just power switches, with the goal that the capacitor charging time is autonomous of the load. The capacitor voltage can be controlled at a coveted level without complex voltage control calculation and just utilize the most widely recognized bearer phase-moved sinusoidal pulse width adjustment technique. The operation principle and the charging–releasing trademark investigation are examined in this paper. By utilizing the simulation results we can check the plausibility and viability of the proposed topology.**

## I. INTRODUCTION

In general, multilevel converters are classified into diode-clamped [5], flying capacitor [6], and cascaded multilevel inverter topologies [7]. A topology because of its modularity, particular attention has been given to cascaded multilevel symmetrical structure, and simplicity of control. A cascade inverter can be directly connected in series with the electrical system for static var compensation. Cascaded inverters are ideal for connecting renewable energy sources with an ac grid, because of the need for separate dc sources, which is the case in applications such as photovoltaic's or fuel cells.

Photovoltaic panel, fuel cells batteries, and ultra capacitors are the most common independent sources.

The most attractive features of multilevel inverters are as follows.

1) They can generate output voltages with extremely low distortion and lower dv/dt.

2) They draw input current with very low distortion.

3) They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated [8].

4) They can operate with a lower switching frequency.

A five-level CMI for distributed energy applications is presented. The CMI input ports are connected to a group of batteries, whose characteristics are large size, high cost, and the battery discharging speed limits the continuity of the system. Some solutions to reduce the number of isolated source in the CMI are proposed.

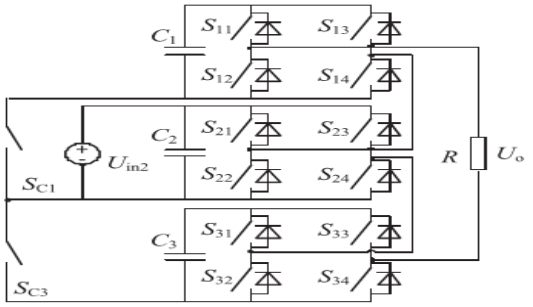
Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications. An important improvement is the "asymmetrical CMI" (ACMI), which can generate the same number of levels with fewer power supplies [10]. ACMI increases the power quality, but they lose modularity and still need more than one isolated sources. To eliminate the dc sources of the auxiliary converters, the system uses a high-frequency link (HFL), based on a square-wave generator and a multiwinding toroidal transformer. An alternative option without transformers is to replace all the separate dc sources feeding the H-bridge cells with capacitors, leaving only one H-bridge cell with a real dc voltage source.

A simple capacitor voltage regulation constraint is derived which can be used in optimization problems for harmonic minimization or harmonic mitigation to guarantee capacitor voltage regulation in all load condition [7]. A new control method, phase-shift modulation, is used to regulate the voltage of the capacitors replacing the independent dc source. The method is robust and does not incur much computational burden [8]. The proposed dc-voltage-ratio control [9] is based on a time-domain modulation strategy that avoids the use of inappropriate states to achieve any dc voltage ratio.

The following are the three associated problems of this topology: 1) regulating the voltage across the capacitors makes the controller design complex, 2) the charging circuit contains the load. Thus, the charging time and the capacitor voltage are affected by the load variation, and 3) the charging–discharging characteristics and efficiency issues of the capacitor are not fully discussed. The efficiency of switched-capacitor in dc–dc converters has been a widely debated issue among researchers [8]–[9]. The efficiency of a RC circuit under different conditions in the charging and discharging operation is analyzed systematically.

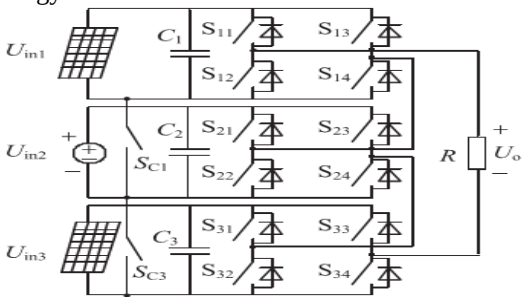
In this paper, a novel cascaded seven-level inverter topology with a single input source integrating switched-capacitor techniques is proposed. The proposed topology consists of a

charging circuit and three H-bridge inverter units, as shown in Fig. 1(a).




(a)

The reliable source port Uin2 can charge capacitor C1 orC3 through the charging switched-capacitor techniques, the different H-bridges can share the input source; thus, the redundancy of the topology is enhanced.




(b)

Fig. 1. Topologies of the proposed inverter. (a) The novel single dc source cascaded seven-level inverter. (b) Three-input cascaded seven level inverter for PV systems.

## II. MODULATIONSTRATEGY

Different multilevel modulation techniques have been presented. For the CMI, CPS-SPWM is the most common strategy [1], with an improved harmonic performance. The CPS-SPWM associates a pair of carriers to each cell of the CMI, and a phase shift among the carriers of the different cells is introduced. In this way, a stepped multilevel waveform is originated. There are some interesting features and advantages: 1) The output voltage has a switching pattern with 2Ntimes the switching frequency (where N is the number of cells). Hence, better total harmonic distortion (THD) is obtained at the output, using 2Ntimes lower frequency carriers. 2) Since all the cells are controlled with the same reference and same carrier frequency, the power is evenly distributed among the cells across the entire modulation index. 3) For the single-supply CMI using capacitors, the advantage is that the capacitors are properly charged without complex voltage balancing control algorithm. The level-shifted SPWM has better output voltage harmonic profile since all the carriers are in phase compared to CPSPWM. However, this method is not preferred for CMI, since it causes an uneven power distribution among the different cells.

Space vector modulation (SVM) exhibits features of good dc-link voltage utilization, better fundamental output voltage, better harmonic performance, and easier implementation in digital signal processor. In this paper, CPS-SPWM is performed to obtain the sinusoidal output voltage in the single-supply cascaded seven-level inverter, and the capacitors are charged by introducing charging switch pairs every cycle. To some extent, capacitor voltageUC1 andUC3are regarded as constants, and the three H-bridge inverter cells share balanced power.

The waveforms of the driving signal are given in Fig. 2. Six-way phase-shifted triangular carrier voltages and one-way sinusoidal modulation wave are required for the CPS-SPWM scheme. Z1,−Z1,Z2,−Z2,Z3, and −Z3 are the carrier signals forS11,S13,S21,S23,S31, and S33, respectively, and TS is the carrier period. A straight line with value m(0<m<1) can be substituted for the modulation wave in a carrier cycle, where the carrier frequency is significantly greater than the modulation frequency. The power switches are turned ON when the corresponding carrier wave signal is less than the modulation sine wave m.

TABLE I
OPERATINGSTATUS OFEACHSWITCH

| | | $S_{11}$ | $S_{13}$ | $S_{21}$ | $S_{23}$ | $S_{31}$ | $S_{33}$ | $S_{C1}$ | $S_{C3}$ |
|---|---|---|---|---|---|---|---|---|---|
| Charging status | Status 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| | Status 2 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| | Status 3 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| | Status 4 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| | Status 5 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| | Status 6 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| Discharging status | Status 7 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| | Status 8 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| | Status 9 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| | Status 10 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| | Status 11 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| | Status 12 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| | Status 13 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | Status 14 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| | Status 15 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | Status 16 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| | Status 17 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Status 18 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| | Status 19 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| | Status 20 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

## III. CAPACITORCHARGING ANDDISCHARGING CHARACTERISTICANALYSIS

### A. Capacitor Charging State Analysis

Through the charging switch and H-bridge switches,$C_1$ and $C_3$ can be charged by the reliable source $U_{in2}$ . From Status 1, Status 2, and Status 3 in Table I, we can see that there is only one charging path forC1. In other words, the capacitor charging

currentiC1only goes throughS21 andS13,as drawn in red color in Fig. 3.

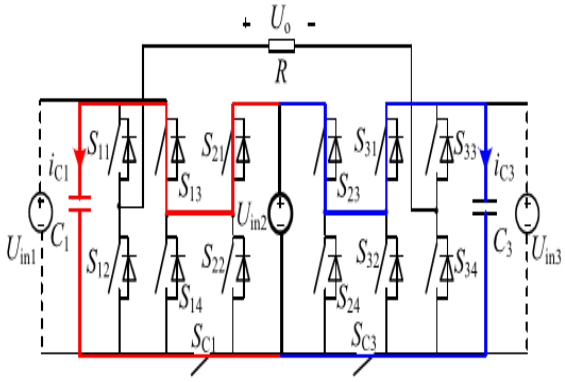
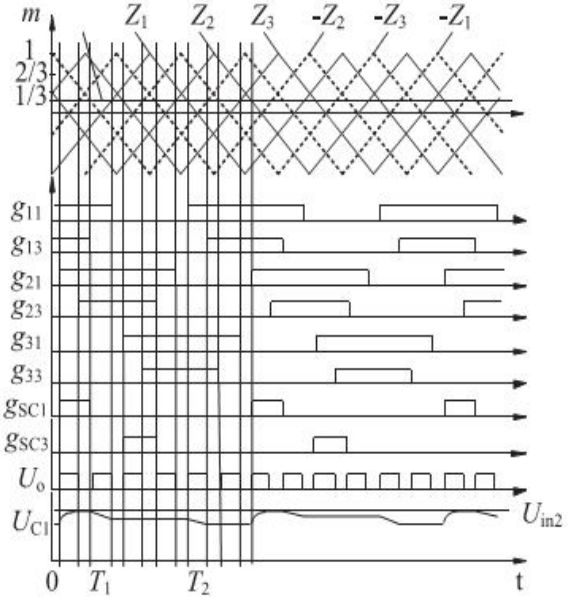



Fig. 3. Equivalent charging circuit forC1 andC3

According to Status 4–Status 6, we can see that charging currentiC3flows throughS23andS31. The equivalent charging circuit for C3 is shown in blue color in Fig. 3.

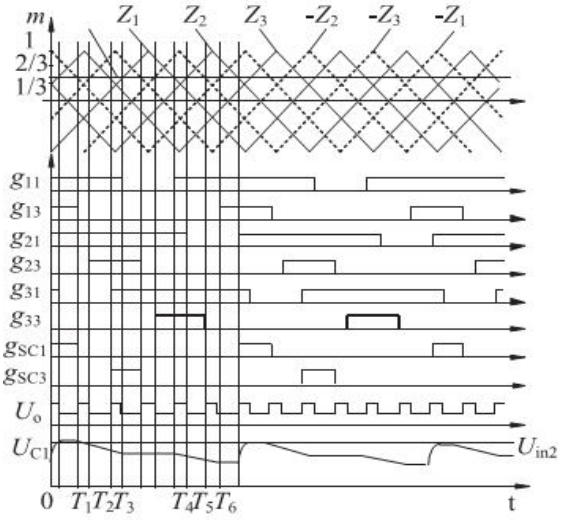
**B. Capacitor Charging Time Analysis**

The capacitor charging time is related to the modulation sine wave value m. For simplicity, the charging time for C1 is taken as an example to have a detailed analysis.

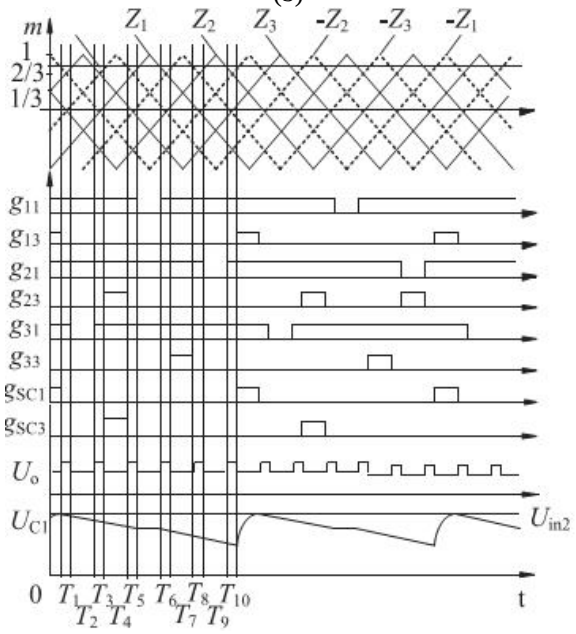



(a)

At this stage, the falling edge of g13and the rising edge ofg21move forward or backward with the variation in m. However, the overlapping portions of g13andg21remain unchanged; thus, the charging time remains TS/6. The output voltage of the inverter is 0 orUin2 when m∈(0, 1/3),as illustrated in Fig. 2(a), and Uin2 or 2Uin2 when m∈ (1/3, 2/3), as illustrated in Fig. 2(b). When m∈(2/3, 1),S21 is turnedOFFafterS13, as illustrated in Fig. 2(c).




(b)




(c)

Fig. 2. Waveforms of the driving signal when CPS-SPWM is employed.
(a)m∈(0,1/3)(b)m∈(1/3,2/3).(c)m∈(2/3,1). Fig. 2(a)and(b).

The charging time is (1−m)TS/2, and the output voltage of the inverter is 2Uin2 or3Uin2 and the capacitor voltageUC1would decrease drastically if the modulation wave is increased to 1; however, it would recover in time if the modulation wave is decreased. Due to the symmetry, the charging time and the output voltage can be easily derived with m<0. Table II gives the charging time and the output voltage in different m.

TABLE II
CHARGINGTIME AND OUTPUTVOLTAGE INDIFFERENT m

| Modulation value $m$ | Charging time | Output voltage |
|---|---|---|
| $-1 < m < -2/3$ | $(1-\lvert m \rvert)T_S/2$ | $-3U_{in2}$, $-2U_{in2}$, |
| $-2/3 < m < -1/3$ | $T_S/6$ | $-2U_{in2}$, $-U_{in2}$ |
| $-1/3 < m < 0$ | $T_S/6$ | $-U_{in2}$, 0 |
| $0 < m < 1/3$ | $T_S/6$ | 0, $-U_{in2}$ |
| $1/3 < m < 2/3$ | $T_S/6$ | $U_{in2}$, $2U_{in2}$ |
| $2/3 < m < 1$ | $(1-m)T_S/2$ | $2U_{in2}$, $3U_{in2}$ |

**C. Capacitor Discharged Bus Voltage Analysis**

To some extent, bus voltages UC1and UC3 remain stable. However, they will fluctuate frequently because of the charging or discharging of the capacitor. The influencing factors ofUC1 andUC3are illustrated as follows. For simplicity, the following assumptions are made: 1) the initial values ofUC1andUC3are Uin2 before discharging; 2) the capacitance of the capacitorC1 andC3isCand the load resistance is R. There are four discharging states forC1 in a modulation cycle, which are described as follows.

**State I: Capacitor C1 operates individually.**

S11, S14, S22, S24, S31, andS33are turned ON simultaneously for Status 7 (S11, S14,S21,S23,S32, and S34areONfor Status 8). The equivalent circuit of Status 7 is shown in Fig. 4(a).UC1 can be expressed as

$$u_{C1}(t) = U_{in2}e^{-\frac{t}{RC}}$$

**StateII CapacitorC1and Uin2 operate simultaneously.**

S11, S14, S21, S24,S31, andS33are turned ON simultaneously for Status 9 (S11,S14,S21,S24,S32, and S34areONfor Status 10). The equivalent circuit of Status 9 is shown in Fig. 4(b).UC1 is provided by

$$u_{C1}(t) = U_{in2}\left(2e^{-\frac{t}{RC}} - 1\right)$$

**State III: Capacitors C1 and C3 operate simultaneously**.

S11, S14, S22,S24,S31, andS34are turned ON simultaneously for Status 11 (S11, S14,S21,S23,S31, andS34areONfor Status 12). The equivalent circuit is shown in Fig. 4(c). UC1can be expressed as

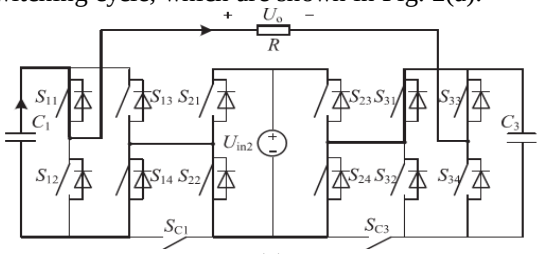
$$u_{C1}(t) = U_{in2}e^{-\frac{2t}{RC}}$$

**State IV: CapacitorsC1, C3, and Uin2 operate simultaneously**.

S11, S14, S21, S24, S31, andS34are turned ON simultaneously for Status 13. The equivalent circuit is shown in Fig. 4(d). UC1 is provided by

$$u_{C1}(t) = U_{in2}\left(\frac{3}{2}e^{-\frac{2t}{RC}} - \frac{1}{2}\right)$$

The analysis above reveals that the proposed converter has four discharging states. For convenience, the discharging time intervals that belong to the same state are regarded as one continuous discharging time. 1) When m∈[0, 1/3), there are two discharging time intervals in a switching cycle, which are shown in Fig. 2(a).

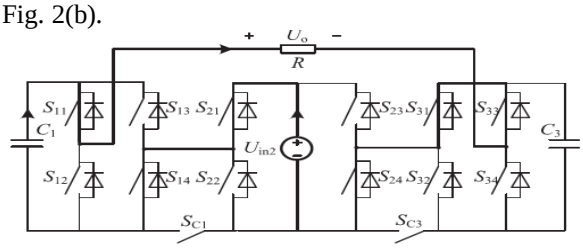



(a)

The two time intervals can be deduced easily asT1 =T2 =m/(2fS). According to (1), the voltage variation acrossC1can be expressed as

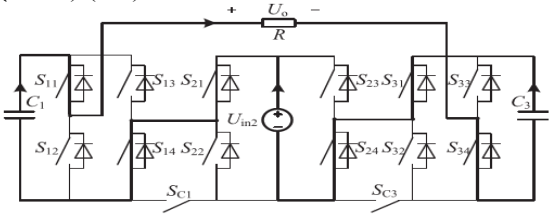
$$\Delta u_1 = U_{in2} - U_{in2}e^{-\frac{m}{fsRC}}$$

2) When m∈[1/3, 2/3), there are six discharging time intervals in a switching cycle, which are shown in Fig. 2(b).




(b)

Capacitor C1 and Uin2 discharge simultaneously during T1 and T6. Capacitor C1 discharges individually during T2 and T5. Capacitors C1andC3discharge simultaneously duringT3andT4. The time intervals can be achieved easily as follows:T1 =T3 =T4 = T6 = (3m−1)/(6fS),T2 =T5 =(2−3m)/(6fS).




(d)

Fig. 4. Capacitor discharging states. (a)C1 operates individually. (b)C1 andUin2 operate simultaneously. (c)C1 andC3 operate simultaneously. (d)C1,C3, and Uin2 operate simultaneously

In reference to (1) to (3), the voltage variation acrossC1 can be expressed as

$$\Delta u_{21} = 2U_{in2}\left(1 - e^{-\frac{3m-1}{3f_SRC}}\right) \quad (6)$$

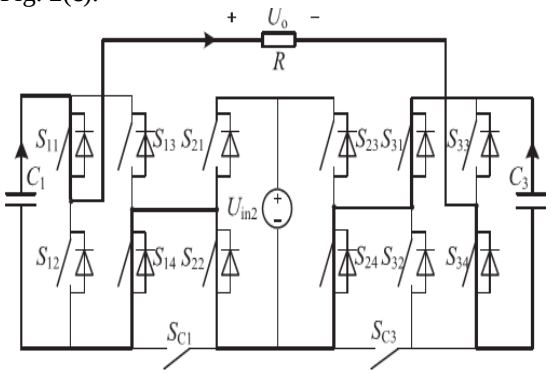
$$\Delta u_{22} = U_{in2}\left(1 - e^{-\frac{2-3m}{3f_SRC}}\right) \quad (7)$$

$$\Delta u_{23} = U_{in2}\left(1 - e^{-\frac{6m-2}{3f_S RC}}\right) \quad (8)$$

From (6) to (8), we obtain

$$\Delta u_2 = \Delta u_{21} + \Delta u_{22} + \Delta u_{23}$$
$$= U_{in2}\left(4 - 2e^{-\frac{3m-1}{3f_S RC}} - e^{-\frac{2-3m}{3f_S RC}} - e^{-\frac{6m-2}{3f_S RC}}\right) \quad (9)$$

3) When m∈[2/3, 1), there are ten discharging time intervals in a switching cycle, which are shown in Fig. 2(c).




(c)

Capacitors C1,C3, and Uin2 discharge simultaneously during T1,T3,T5,T6,T8, and T10. Capacitor C1 and Uin2 discharge simultaneously duringT2 and T7. According to (2)–(4), the voltage variation across C1 is provided by

$$\Delta u_{31} = \frac{3}{2}U_{in2}\left(1 - e^{-\frac{6m-4}{f_S RC}}\right) \quad (10)$$

$$\Delta u_{32} = 2U_{in2}\left(1 - e^{-\frac{1-m}{f_S RC}}\right) \quad (11)$$

$$\Delta u_{33} = U_{in2}\left(1 - e^{-\frac{2-2m}{f_S RC}}\right) \quad (12)$$

From (10) to (12), we obtain

$$\Delta u_3 = \Delta u_{31} + \Delta u_{32} + \Delta u_{33}$$
$$= U_{in2}\left(\frac{9}{2} - \frac{3}{2}e^{-\frac{6m-4}{f_S RC}} - 2e^{-\frac{1-m}{f_S RC}} - e^{-\frac{2-2m}{f_S RC}}\right) \quad (13)$$

The capacitor voltage variation Δu is a function of modulation value m, switching frequency $f_S$, load resistance R, capacitance C1, and source voltage Uin2 Δu decreases when switching frequency fS, load resistance R, or capacitanceC1 increases. The capacitor voltage variation for different modulation values and frequencies under the condition of Uin2 = 136 V, R=50Ω,andC= 4700μFis drawn in Fig. 5.

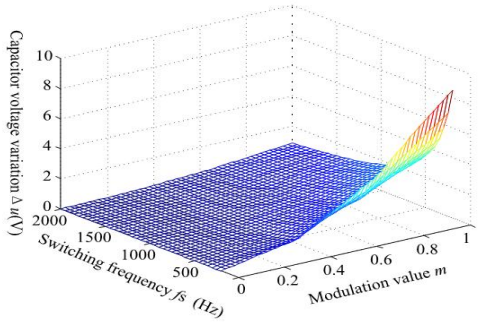



Fig. 5. Scope of capacitor voltage variation at different modulation values and frequencies

A large switching frequency should be selected to achieve a small capacitor voltage ripple and improve the steady-state performance of the system.

## IV. CURRENT ANDVOLTAGE ONCHARGINGSWITCH

### A. Charging Current and Loss Analysis

Given thatUC1andUC3are almost zero in the initial state, the charging current would reach the maximum at system startup. Excessive spike charging current will damage the capacitor and cause the converter to exhibit inefficiency. A current limitation resistor is normally utilized to reduce the charging current but is not discussed in the following analysis. The charging circuit forC1[see Fig. 6(a)]contains only power switches and capacitor, which can be represented by a RC circuit [see Fig. 6(b)].

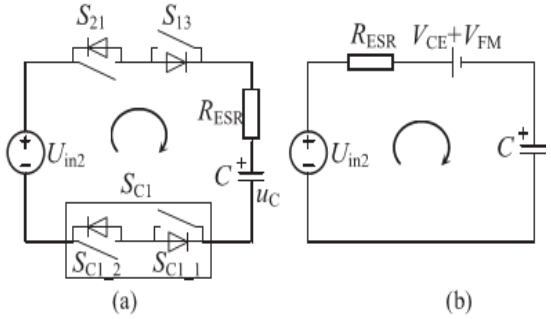



Fig. 6. Circuit and equivalent circuit of the charging process. (a) Charging circuit. (b) Equivalent charging circuit

For simplicity, the following assumptions are made: 1) all power switches are insulated-gate bipolar transistors (IGBTs), 2)VCE is the sum of the forward conduction voltage for S21and SC11 and VFM is the sum of the diode forward voltage forS13andSC12, and 3)RESR represents the equivalent series resistance (ESR) of the capacitor. The capacitor voltage waveforms of charging process are illustrated in Fig. 7.

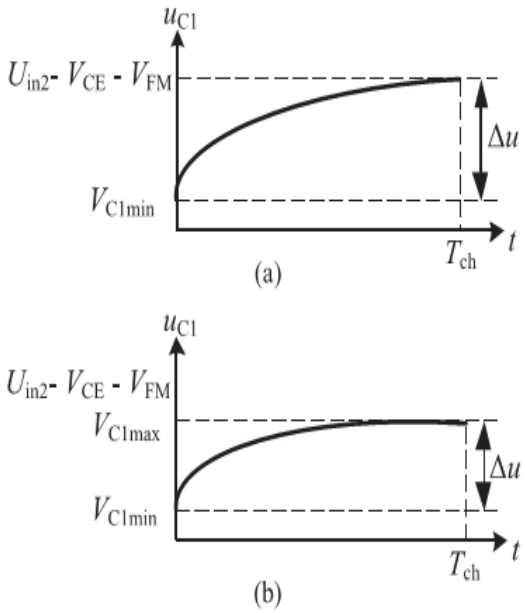



Fig. 7. Capacitor voltage waveforms of charging process. (a) Full charging. (b) Partial charging.

VC1mindenotes the initial capacitor voltage andVC1maxrepresents the final capacitor voltage. The capacitor charging process can be classified into two conditions, namely, full charging and partial charging. In [24], full charging is defined as one that has a charging time period longer than four times the charging time constant, i.e. $T_{ch} \geq 4\tau ch$, and partial charging corresponds to $T_{ch} < 4\tau ch$, where τch =RESRC. In full charging, the capacitor is charged to the steady-state voltage Uin2 −VCE−VFM,as shown in Fig. 7(a). In partial charging, the capacitor is charged to a voltage less than Uin2 −VCE−VFM,as shown in Fig. 7(b). The instantaneous capacitor voltage and current can be given by

$$\begin{cases} u_{C1}(t) = V_{C1max} + (V_{C1min} - V_{C1max})e^{-\frac{t}{R_{ESR}C}} \\ i_{C1}(t) = \frac{V_{C1max}-V_{C1min}}{R_{ESR}} e^{-\frac{t}{R_{ESR}C}} = \frac{\Delta u}{R_{ESR}} e^{-\frac{t}{R_{ESR}C}} \end{cases} \quad (14)$$

The maximum charging current can be expressed by

$$i_{C1max} = \frac{\Delta u_{max}}{R_{ESR}} \quad (15)$$

From Fig. 5, the capacitor voltage variation Δu is a function of modulation value mat a certain switching frequency fS, load resistance R, capacitance C, and source voltage Uin2 . Δu increases when m increases. Therefore, we get the peak current.

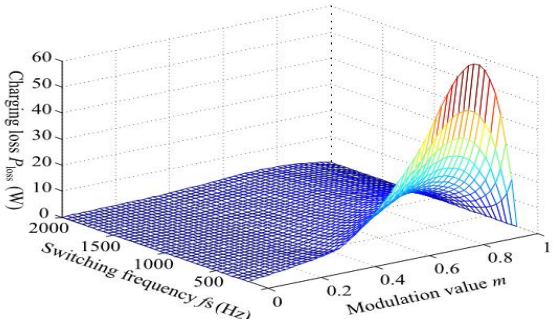



Fig. 8. Extent of charging loss at different modulation amplitudes and
frequencies.

**B. Charging Switch Voltage Analysis**

By introducing the charging-switch pairs, the proposed cascaded seven-level inverter can operate well with only a single dc input source. It is necessary to analyze the charging-switch pair's voltage stress andSC1was taken as an example for the voltage analysis. There are four voltage states forSC1in a modulation cycle, which are described as follows.

State I: S13,S21, and SC1are turned ON. The positive sides ofC1 and Uin2 are connected directly. Input source Uin2 can chargeC1by introducingSC1, as shown in Fig. 3. The voltage ofSC1is zero.

State II: S13 andS22 are turned ON, and SC1is turned OFF. The voltage ofSC1is –SC1,as shown in Fig. 9.

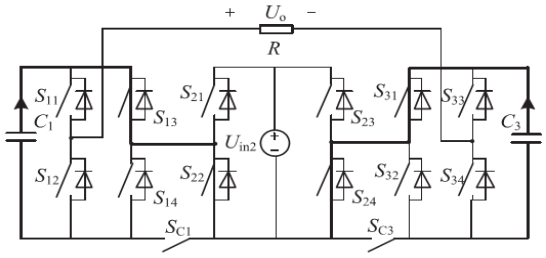
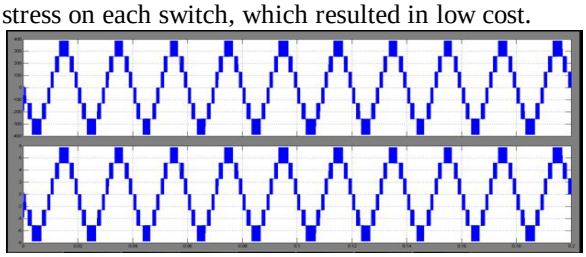



Fig. 9. Voltage ofSC1in state II.

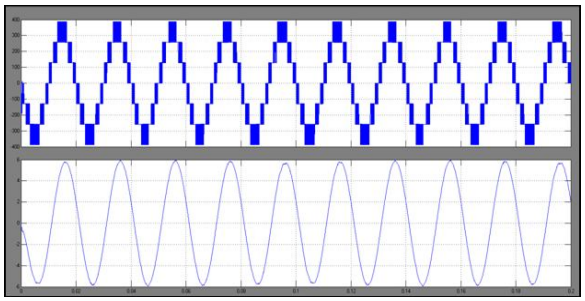
State III: In Fig. 4(b)and (d),S14andS21are turned ON, and the voltage ofSC1is Uin2 .

State IV: In Fig. 4(a)and(c), S14andS22are turned ON and the voltage ofSC1is zero.

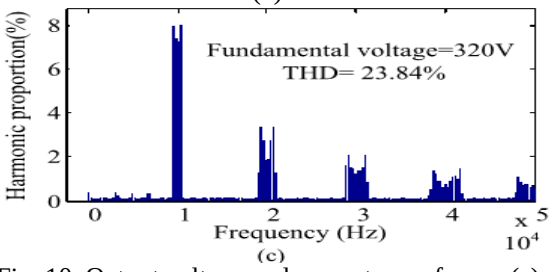
States I–IV indicate that the voltage ofSC1is 0, the capacitor voltageUC1or the source voltageUin2. Therefore, the proposed converter has low voltage stress on each switch, which resulted in low cost.



(a)



(b)




(c)

Fig. 10. Output voltage and current waveforms. (a) At resistive load.
(b) At inductive load. (c) THD value of the output voltage.

The output voltage and current waveforms for resistive and inductive load are given in Fig. 10. The output current lags behind the voltage at inductive load.

## V. SIMULATION VERIFICATIONS

### A. Simulation Results

The simulation parameters of the proposed converter are given in Table III.

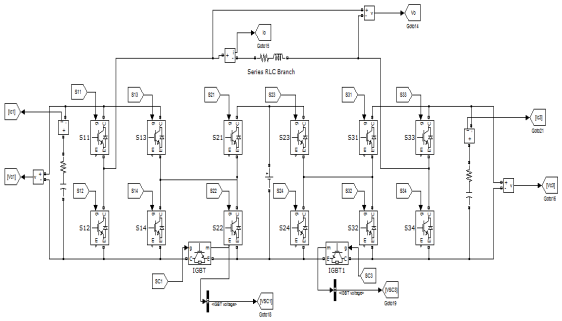
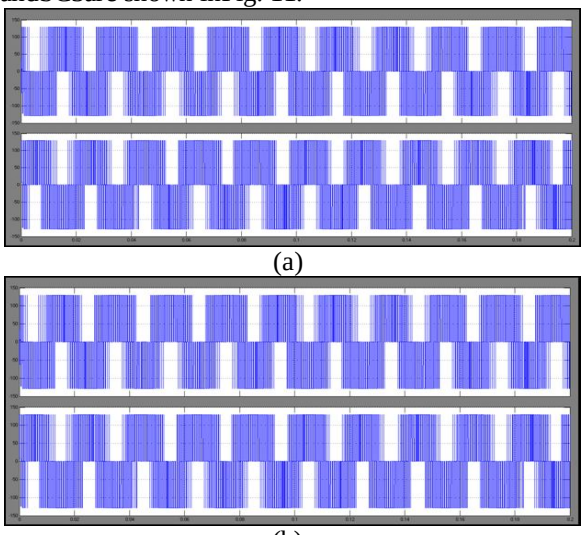


Fig. Block diagram of simulation

TABLE III
SYSTEMSIMULATION PARAMETERS

| Circuit parameters | Value |
|---|---|
| $U_{in2}$ | 136 V |
| fs | 1.667 kHz |
| $R$ | 50 Ω |
| $L$ | 60 mH |
| $C_1/C_3$ | 4700 $\mu$F |

The THD value ofuOis 23.84%. The ideal voltage waveforms of the charging-switch pairsSC1 andSC3are shown inFig. 11.



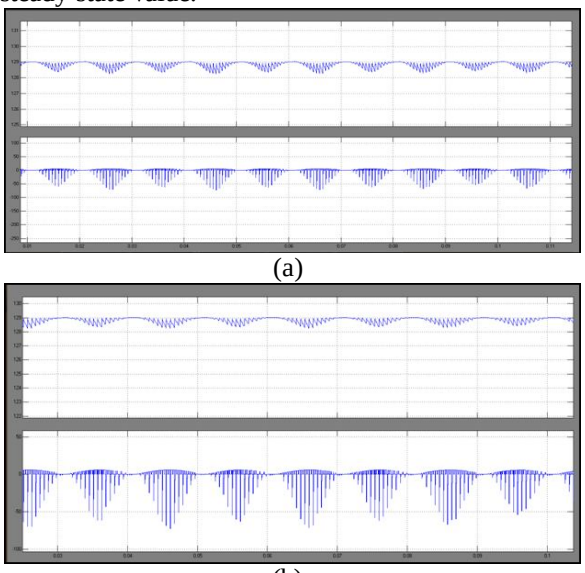
(a)

(b)

Fig. 11. Voltage waveforms of the charging-switch. (a)SC1.(b)SC3.

The capacitor voltage and the charging current waveforms of capacitorsC1 with the ESR value of5mΩin the full charging process are shown in Fig. 12(a).

The waveforms with the ESR value of 200 Mω in the partial process are illustrated in Fig. 12(b).Due to a large RESR, the peak charging current can be limited. However,uC1 cannot reach the steady-state value.



(a)

(b)

Fig. 12. Capacitor voltage and the charging current waveforms of capacitors C1.(a)RESR=5mΩ. (b)RESR= 200 mΩ.

the charge–discharge process is so complicated that we cannot get the specific expression of the peak current.

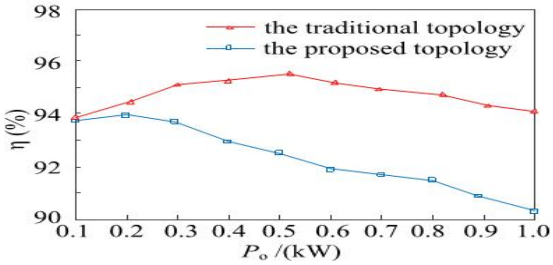



Fig. 16. Efficiency versus power in the proposed and traditional
Topologies

## VI. CONCLUSION

A novel single dc source cascaded seven-level inverter incorporating exchanged capacitor strategy was produced in this paper. In the proposed topology, the transformerless charging circuit just contains power switches and capacitors, and the charging time is free of the load. The operation principle and the charging– releasing trademark examination were explored top to bottom. With the normal CPS-SPWM methodology, the sinusoidal output voltage can be all around got. Additionally, the capacitors are legitimately charged without complex voltage adjusting control calculation. The pinnacle charging current and the charging misfortune can be decreased with fitting circuit parameters. The proposed topology has the highlights of particularity, ease, and effortlessness of control and makes it attractive in dc– air conditioning power applications. The proposed inverter is likewise appropriate for photovoltaic-battery multi-input application with high excess.

## REFERENCES

[1] S. Kouroet al., "Recent advances and industrial applications of multilevel converters,"IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[2] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters; state of the art, challenges, and requirements in industrial applications," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2581–2596, Aug. 2010

[3] J. Dixon, J. Pereda, C. Castillo, and S. Bosch, "Asymmetrical multilevel inverter for traction drives using only one dc supply," IEEE Trans. Veh. Technol., vol. 59, no. 8, pp. 3736–3743, Oct. 2010.

[4] S. Lu, K. A. Corzine, and M. Ferdowsi, "A unique ultracapacitor direct integration scheme in multilevel motor drives for large vehicle propulsion," IEEE Trans. Veh. Technol., vol. 56, no. 4, pp. 1506–1515, Jul. 2007.

[5] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters,"IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219–2230, Jul. 2010.

[6] M. Khaazraei, H. Sepahvand, K. A. Corzine, and M. Ferdowsi, "Active capacitor voltage balancing in single-phase flying capacitor multilevel power converters,"IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 769– 778, Feb. 2012.

[7] I. Ahmed and V. B. Borghate, "Simplified space vector modulation technique for seven-level cascaded H-bridge inverter,"IET Power Electron., vol. 7, no. 3, pp. 604–613, Apr. 2014.

[8] Y. H. Liao and C. M. Lai, "Newly-constructed simplified single-phase multi-string multilevel inverter topology for distributed energy resources," IEEE Trans. Power Electron., vol. 26, no. 9, pp. 2386–2391, Sep. 2011.

[9] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "A transformerless battery energy storage system based on a multilevel cascade PWM converter," inProc. 39th Annu. IEEE Power Electron. Conf., 2008, pp. 4798–4804.

[10] M. N. A. Kadir and Z. F. Hussien, "Asymmetrical multilevel inverter: Maximum resolution for H-bridge topology," inProc. Int. Conf. Power Electron. Drivers Syst., 2005, pp. 1068–1071.

**VASUDEV RATHOD**
Completed B.E in Electrical & Electronics Engineering in 2015 from VTU UNIVERSITY, KARNATAKA and Pursuing M.Tech form Ballari institute of Technology and management Engineering College Affiliated to VTU, Belagavi, and Karnataka, India. Area of interest is Power Electronics.
E-mail id;vasurathod699@gmail.com