DESIGN OF TRACK AND HOLD AMPLIFIER FOR 55 GHZ BANDWIDTH

K.Rajasekhar Reddy[1]*,PG Scholar, VLSI, St.John's college of Engineering and Technology, Kurnool, A.P.*
U.Veeresh[2]***,****Assistant Professor, Dept. of ECE, St.John's college of Engineering and Technology, Kurnool, A.P.*
T.Chakrapani[3]***,*** *Associate Professor, Dept. of ECE, St.John's college of Engineering and Technology, Kurnool, A.P.*
K.Sudhakar[4]*, Professor, Dept. of ECE, St.John's college of Engineering and Technology, Kurnool, A.P.*

Abstract: **An open-loop 25-GS/s track-and-hold amplifier (THA) using fully-differential architecture to mitigate common-mode noise and suppress even-order harmonics is presented. Large-signal measurements show a 3-dB corner frequency of 55 GHz, which enables a performance sufficient for time-interleaved analog-to-digital converter systems operating above 100 GS/s. CMOS switch and dummy switches are adopted to achieve high speed and good linearity. A cross-coupled pair is used in the input buffer to suppress the charge injection and clock feed through. Both the input and output buffers use an active inductor load to achieve high signal bandwidth. The THA is realized with 0.18 µm SiGe Bi-CMOS technology using only CMOS devices at a 1.8 V voltage supply and with a core area of 0.024 mm2. The measurement results show that the SFDR is 32.4 dB with a 4 GHz sine wave input at a 20 GSps sampling rate, and the third harmonic distortion is −48 dBc. The effective resolution bandwidth of the THA is 12 GHz and the figure of merit is only 0.028 mW/GHz.**

Index Terms—High-speed sampling, sampling circuit, switched capacitor (SC), time interleaving, track-and-hold amplifier (THA).

I. INTRODUCTION

One fundamental concern for such ADCs is the accessibility of testing circuits with sufficient information data transmission to help Nyquist-rate change for the interleaved ADC frameworks. Time-interleaved simple to-computerized converter (ADC) frameworks executed in present day CMOS advances have empowered radical increments in testing rates and have prompted frameworks with up to 100 GS/s. Track-and-hold amplifiers (THAs) with small-signal input bandwidths up to 50 GHz have been reported in In P, and SiGe technologies, but the combination of InP/SiGe THA circuits and CMOS ADCs is very difficult to package and is expensive. THAs in InP and SiGe are usually implemented using the switched-emitter follower (SEF) topology, which typically results in high power consumption. The CMOS equivalent to SEF, the switched source-follower topology, is frequently used for high-speed applications but suffers from low input compression due to the reduced supply voltages in modern CMOS processes.

By increasing the number of interleaved ADCs, the overall sampling rate of the ADC system can be increased, while the speed requirements for the single ADCs remain unchanged. This works as long as it is possible to take samples of the high-speed input signal and process them with alternating ADCs at a lower speed. In this way, the task of processing the full speed input signal is shifted from the ADC to the sampling circuit, in this case, the THA. In order to sample signals at higher frequencies, THA circuits need larger bandwidth. The basic principle in time-interleaved ADC systems is that several independent ADCs alternate in sampling the common input signal.

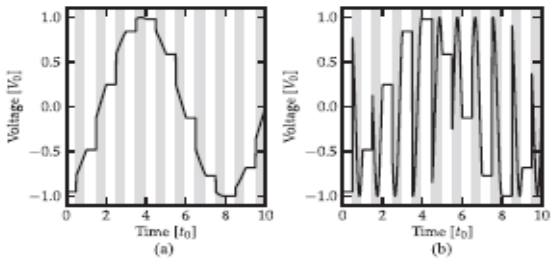


Fig. 1: Output signals of an ideal THA for different input frequencies. The ratio of input signal frequency

to sampling rate is 0.12 for (a) and 1.12 for (b). Signals such as (b) are used in time-interleaved systems. Tracking periods are marked in gray.

This brief presents the first SC THA circuit that exploits designed frequency compensation for the T/H core. Due to this design method, the small-signal input bandwidth is enhanced by almost 30%.

II. RELATED WORK

THA CIRCUITS IN TIME-INTERLEAVED ADC SYSTEMS

Fig. 1 shows the output of an ideal THA for two different input frequencies f. The ratio between input frequency and sampling rate, i.e., f/fs, is 0.12 for (a) and 1.12 for (b). The signal in (b) is an example for a THA that is used in the context of time interleaving, because the input frequency is higher than the Nyquist frequency. In order to reconstruct all information of the input signal in such a case, the outputs of multiple time interleaved THAs are required. The hold plateaus of (a) and (b) are the same, but the signal in (b) changes much faster during the tracking periods.

If the bandwidth of the THA is not sufficient for a given input signal, the amplitude at the output will decrease and distortions will grow, leading to degradations in the signal-to-noise-and-distortion ratio (SNDR). The goal of the presented sampling circuit is to partially compensate for the inherent low-pass behavior of SC THAs and thus increase the input bandwidth.

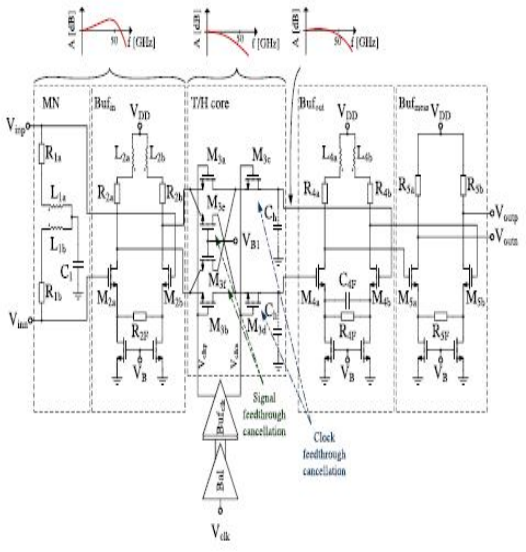


Fig. 2. Schematic of the complete THA with matching network MN, input buffer Buf-in, T/H core, output buffer Buf-out, and measurement equipment driver stage Bufmeas. The top of the figure indicates the frequency-dependent signal attenuation of the input stages and sampler.

The fundamental power shows a 3-dB corner frequency of 55 GHz for both input signal amplitudes of 400 and 800 mV.

Fig. 2 shows the schematic of the presented THA. It consists of an input matching network MN, an input buffer Bufin, the T/H core, an output buffer Bufout, and an additional driver stage Bufmeas, which is required for circuit characterization only. The T/H core with the switch transistors M3a,b and the hold capacitance Ch implements clock and signal feed through cancellation. Ch is a 7-fF capacitance, which consists of the input capacitance of the subsequent buffer stage and metal wiring. Clock feed through is compensated by the transistors M3c,d, which are controlled by the inversed clock signal Vclkn [9]. Exploiting the cross coupling of the differential input signal, the transistors M3e,f compensate for signal feed through in the hold mode.

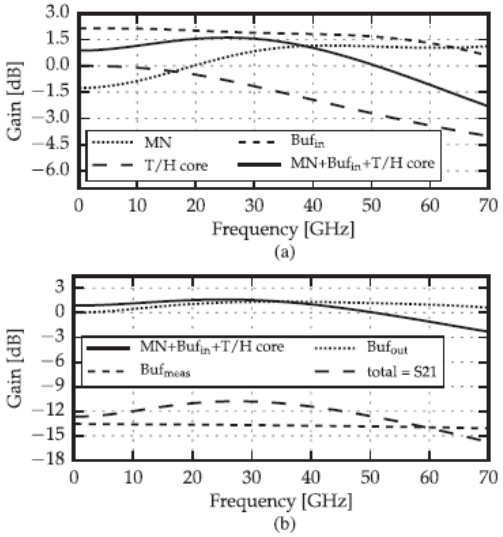


Fig. 3: Simulated small-signal voltage gain of all circuit blocks. For this characterization, the THA is kept in track mode. (a) Input circuitry up to the T/H core. The gain of the MN is relative to 50-Ω input matching. (b) Circuitry following the T/H core. Adding the total gain of all blocks yields S21.

III. EXISTIN METHOD

SiGe Technology: The SiGe HBT technology used for the present THA is a

commercially-available 130 nm BiCMOS process, and features high-performance npn SiGe HBTs with a peak fT / fMAX of 200/280 GHz, ASIC compatible 1.3 V Si CMOS, and a full suite of passive elements, including metal insulator-metal (MIM) capacitors and thin-film resistors. Five levels of full copper interconnects are available, along with two thick top layer aluminum metalization layers to enable high-Q inductors and robust transmission line designs.

THA Design

` The traditional THA with a SEF configuration has some drawbacks that affect the operation of the THA and degrade performance. One major limitation is the hold mode feed through interference that causes large pedestal error in the voltages on the hold capacitors. This problem comes from the signal coupling from the input amplifier through the non-linear emitter-base junction capacitance of the bipolar transistor in the SEF. To suppress this- feed through interference, a feed through attenuation network is introduced in the present THA, and the block diagram is shown in Figure 4.

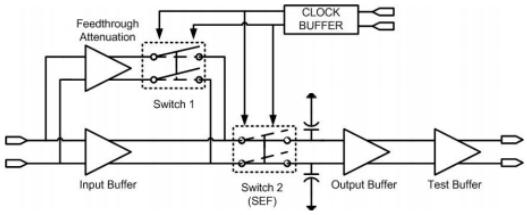


Fig. 4. The SiGe THA block diagram

IV.PROPOSED METHODOLOGY

For small-signal characterization, the T/H core shows low-pass behavior in track mode with a simulated 3-dB corner frequency of 53.9 GHz. To increase the THA bandwidth, the input matching network MN and buffer Bufin are used to peak the input signal of the T/H core at higher frequencies by applying shunt peaking. While inductive peaking is commonly used to increase amplifier bandwidth by adding an additional zero to the transfer function, it serves another purpose in the presented design: the peaking generates an amplitude overshoot at higher frequencies, which is tailored to compensate for the attenuation of the T/H core. The small-signal transfer characteristics of all circuit blocks are shown in Fig. 3(a). For this simulation, the THA is kept in track mode. The peaking of Bufin creates no overshoot in the frequency response, which helps to keep the group delay and transient overshoot low. The buffer bandwidth is increased by 87%, from 45.1 to 84.5 GHz. This increase reaches the optimum predicted by for a purely capacitive load, but is helped in this specific case by the resistive parasitic of the T/H core. By increasing the circuit input impedance, the inductors L1a,b change the input matching over frequency and thus change the input voltage amplitude in comparison with 50-Ω matching.

This increases the input voltage by 2.4 dB at 45 GHz compared with its dc value. As a result, the combined transfer function ofMN, Bufin, and the T/H core shows a simulated 3-dB corner frequency of 68.3 GHz, which is an increase of 27% over the T/H core bandwidth. The main drawbacks of this frequency compensation are additional group delay and transient overshoot in the step response. Both effects are simulated to be unproblematic though: the combination of MN and Bufin induces a maximum group delay of 3 ps and a transient overshoot of less than 5% within one tracking period of 20 ps.

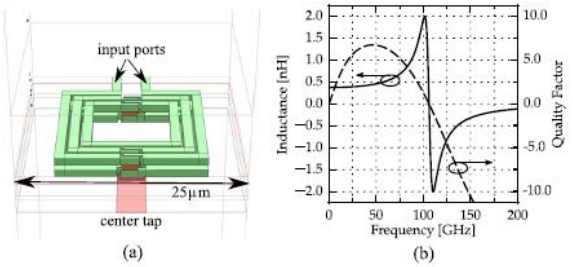


Fig. 5: Simulations of the symmetrical inductor. (a) 3-D image. (b) Inductance and quality factor.

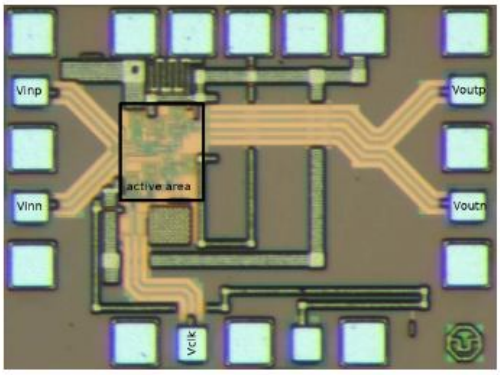


Fig. 6: Chip photograph.

The output buffer Bufout is designed to drive a bank of continuous-time comparators of a flash ADC

implemented in the same technology . To increase the bandwidth, inductive peaking and source degeneration with a bypass capacitor are applied. In the presented circuit, Bufout drives an output buffer, i.e., Bufmeas, which has been implemented to drive the 50-Ω measurement equipment with lowest possible distortion. For this reason, the bandwidth of this buffer exceeds 100 GHz at the cost of a low voltage gain of −13 dB. This low gain is only relevant for measurement purposes, as the buffer is not needed in a full system that implements THAs and ADC cores together. The small-signal behavior of both buffers is shown in Fig. 3(b). Apart from the attenuation, they create a peaking of 1.1 dB in the frequency domain and change the 3-dB corner frequency of the T/H output signal by 1.8%, from 68.3 to 69.5 GHz. In addition to the frequency compensation, one key challenge for the design is the large bandwidth of all signals, with frequencies reaching the millimeter-wave band. In order to accurately predict the circuit behavior at those frequencies, several radio frequency (RF) design techniques have been applied to the presented circuit.

A solid ground plane on the lowest metal layer connects all components and transmission lines to ease modular modeling of components and sub circuits. All key connections and passive components have been investigated with electromagnetic (EM) simulations. The clock, input, and output signals are distributed with patterned ground shield coplanar waveguide transmission lines, which have been modeled with an EM simulator. All employed inductors have been analyzed with the same software. In order to minimize the required area, the inductors are implemented symmetrically and are optimized for small conductor width. The inductors feature a differential inductance of 400 pH, with a physical size of 25 µm × 25 µm.

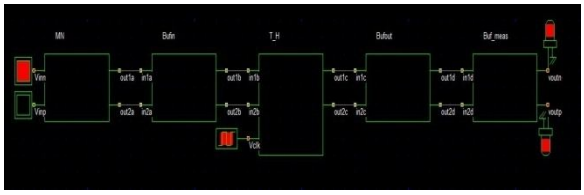
The small size is achieved by using two windings on different metal layers. Fig. 4 shows a three-dimensional (3-D) view of the layout and the frequency-dependent behavior of inductance and quality factor. Despite the use of multiple metal layers, the predicted resonance frequency is 105 GHz, which is sufficiently high for all signals within the bandwidth of the presented circuit. The circuit is robust against moderate process variations in the inductors. Deviations of the inductance of ±10% affect the simulated small-signal bandwidth by no more than ±2%. Since all inductors are used in series connections with resistors, the quality factor is not an important design factor. It reaches a maximum of 7 at 45 GHz. Apart from the RF signals, the dc power distribution network has been modeled with EM software. It is based on zero-Ohm transmission lines, characterized by high conductivity for dc signals and high ac signal attenuation. Such lines isolate very well different circuit blocks, which are connected to the same supply voltage domain. In contrast to local blocking capacitors, they are not susceptible to resonance with series inductances and thus relax the requirements for the connection of external supply and reference voltages.

The exhibited circuit has been actualized in a 28-nm low power computerized CMOS innovation. The chip photo in Fig. 5 demonstrates the kick the bucket size of 0.53mm2, with a dynamic region of 0.03mm2. At an examining rate of 25 GS/s, the chip expends an aggregate power of 73 mW from two supply voltage spaces at 1.4 and 1.75 V. The THA works with the 1.4-V supply, though part of the clock cradle is associated with the 1.75-V space. Amid circuit operation, the gate– source and drain– source voltages of all transistors never surpass the breakdown voltage, which is 1.1 V for the given low-control innovation.

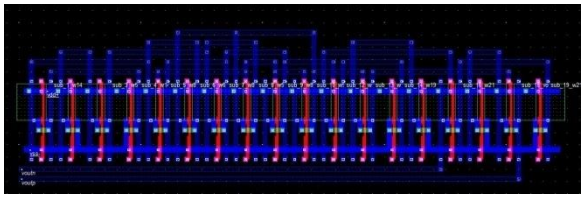
V. EXPERIMENTAL RESULTS

To characterize the performance of the circuit, small-signal measurements with a network analyzer and large-signal measurements with a sampling oscilloscope have been carried out.

SCHEMATIC:

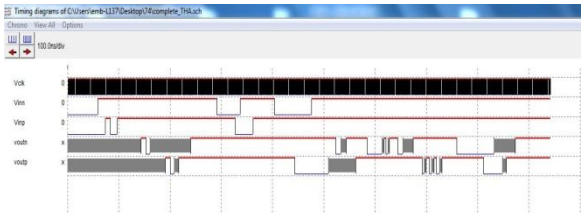


Layout Design:



The presented THA has the highest small- and large-signal bandwidths, even in comparison with designs implemented in dedicated RF technologies such as SiGe and InP circuits. The bandwidth exceeds the sampling rate of 25 GS/s, which makes this THA suited for time-interleaved ADC systems and enables Nyquist-rate operation up to sampling rates of 110 GS/s.

Timing Diagram



The design in the heavily scaled 28-nm CMOS technology allows integration of this THA together with the most recent state-of-the-art ADCs. With an active area of 0.03 mm2 and a power consumption of 73 mW, this circuit combines a small footprint with remarkable energy efficiency.

Comparison Table.

Design	Power
Existing	560mW
Proposed	0.547mW

VI. CONCLUSION

This paper shows the outline, execution, and portrayal of a SC THA in 28-nm low-control CMOS. The SC topology empowers huge flag amplitudes, yet experiences innate low-pass conduct. increasing the amplitude at the contribution of the THA at higher frequencies, it is conceivable to relieve this impact. The displayed THA is the main execution to abuse this rule and show its potential. It employs recurrence remuneration to expand the little flag data transfer capacity by very nearly 30%. To the best of our insight, the examining circuit yields the most elevated data transmission answered to date. At the same time, it permits differential info amplitudes up to 800 mV crest to-top, which outperforms past best in class CMOS THAs in a similar recurrence go by more than a factor of 2, while as yet working at a direct power level of 73 mW. The latest patterns in high-rate ADC plan, which intensely depend on parallelization, make the execution of THAs important, especially regarding data transmission and input adequacy. This concise presents a helpful plan procedure furthermore, usage for this vital segment, which can empower higher rates of operation in the most present day CMOS advancements.

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