A NOVEL FIVE-LEVEL VOLTAGE SOURCE INVERTER WITH SINUSOIDAL PULSE WIDTH MODULATOR FOR MEDIUM VOLTAGE APPLICATIONS BY USING ANN CONTROLLER

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ABSTRACT- A new five-level voltage source inverter (VSI) with sinusoidal pulse width modulator for medium-voltage high-power applications is proposed in this paper by using of ANN. The proposed inverter is based on the upgrade of a four-level nested neutral-point clamped (NNPC) converter. To control and balance the capacitor voltages a novel and simple SPWM techniques is also developed for the proposed converter. This inverter can operate over a wide range of voltages without the need for connecting power semiconductor in series, has high quality output voltage and fewer components compared to other classic five-level topologies. The features and operation of the proposed converter are studied and a simple sinusoidal PWM scheme is developed to control and balance the flying capacitors to their desired values. The performance of the proposed converter is evaluated by simulation and experimental results. By using the simulation results we can analyze the performance of the proposed method under different operating conditions.

INTRODUCTION

Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. For high-power medium-voltage (MV) industrial applications, multilevel converters are the best candidates and this is because multilevel topologies can synthesize near sinusoidal voltage with low harmonic distortion that reduces the size of output filter. These topologies have also low switch stress, reduced common mode voltage, and high voltage capability [1]-[4].

In this paper, a new five-level voltage source converter that is based on the upgrade of a four-level NNPC converter is proposed. This inverter, compared to other classic five-level topologies, can operate over a wider range of voltages without the need for connecting power semiconductor in series and it also has fewer components. The diode clamped converter (DCC), flying capacitor converter (FC), and the cascaded H-bridge (CHB) converter are the most well-known multilevel converter topologies [2] that have been commercialized successfully by major manufacturers. However, these topologies have some drawbacks which limit their applications for more levels. DCC topology with more number of levels is less attractive because of its limitations; 1) dc-link capacitor voltage balance becomes unattainable in higher level topologies with a passive front end, and 2) the number of clamping diodes increases substantially with the voltage level [5]. Flying Capacitor (FC) topology needs to have higher switching frequencies to keep the capacitors properly balanced, whether a self-balancing or a control-assisted balancing modulation method is used. Also the number of flying capacitors increases with the voltage level. Although cascade H-Bridge (CHB) topology can reach higher voltage and higher power levels with modular structure, this topology needs a number of isolated dc sources, an expensive and bulky phase-shifting transformer, and a substantially more number of active devices to achieve a regenerative operation.

• A five-level H-bridge NPC (5L-HNPC) is the H-bridge connection of two classic 3L-NPC phase legs [6]-[8].

• A five-level active NPC (5L-ANPC) is a combination of a 3L-ANPC and 3L-FC, which increases the number of voltage levels [9].

• A five-level diode-clamped converter [5], which has a large number of clamping diodes. This converter has 36 diodes, 12 diodes in each phase. Voltage balancing of the dc-link capacitors is another issue with this topology which has been studied comprehensively in [5].

Recently, a novel four-level nested neutral point clamped (NNPC) converter has been proposed in this paper. The proposed five-level converter mitigates the drawbacks of the previous five-level converters. This converter has the following features;

1. The number of clamping diode has been reduced significantly compared to five-level DCC converter. A five-level DCC converter has 12 diodes in each phase however the proposed topology needs 2 diodes per phase [5].
2. It has fewer flying capacitors compared to five-level FC converter.
3. Unlike 5L-HNPC converter, the proposed converter does not need any isolated DC source that

makes the converter appropriate for regenerative applications.

4. Unlike 5L-ANPC, the voltage stresses of the power switches are the same and they are equal to quarter of the input dc-link voltage[6].

in MATLAB/Simulink environment. The feasibility of the proposed converter is verified by a scale-down prototype converter.

CONVERTER TOPOLOGY

A. Operation of the Proposed Five-Level Voltage Source Inverter

The proposed multilevel topology, as shown in Fig. 1, is based on the upgrade of a four-level nested neutral-point clamped (NNPC) converter.

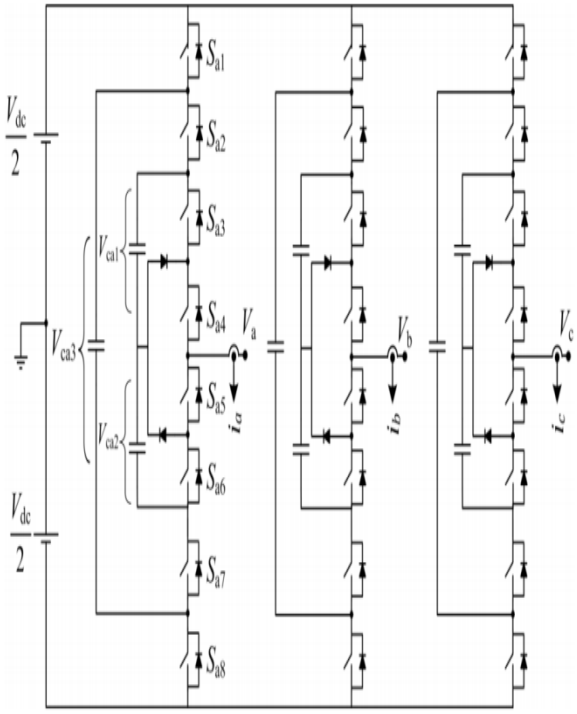

Fig. 1. A new five-level three-phase inverter.

To ensure equally spaced steps in the output voltages, the capacitor Cx1 and Cx2, x=a,b,c are charged to 1/4Vdc and Cx3 is charged to 3/4Vdc

Five output levels are achieved from twelve distinct switching combinations. The list of switching combinations is shown in Table I. It should be noted that the voltage stresses across the switches do not exceed 1/4 of dc-link voltage. Another advantage of the proposed converter is the redundancy in switch combination to generate the output levels[4].

B.SPWM Scheme for the Proposed Five-Level Inverter

One of the most popular modulation scheme in industry applications is Sinusoidal PWM (SPWM). This modulation scheme is based on multicarrier PWM strategy. In this section, a new approach is proposed to use the multicarrier SPWM strategy to generate multilevel output voltage while regulating the voltage of flying capacitors[5]. This approach employs the deviation of the capacitor voltages from their nominal values and based on the converter output current select the best switching state from the available redundant switching states to charge or discharge the capacitors and finally regulate the voltages of capacitors.

In this strategy, four level-shifted triangular carriers with in-phase disposition (IPD) method are employed, where all carriers are in phase and have the same magnitude as shown in Fig.2(a).

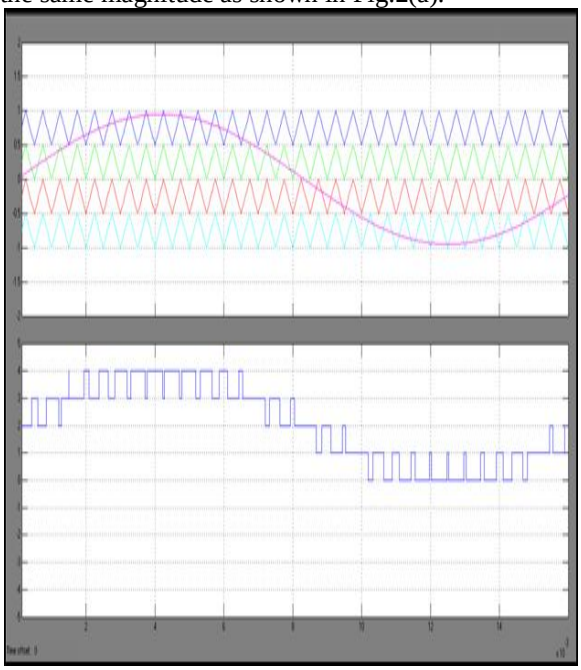

Fig. 2. Level-shifted multicarrier strategy for a five-level inverter. (a) Level shifted multicarrier modulation for a 5L FC-NNPC topology. (b) Desired output levels.

Fig. 2(b) shows the desired output levels which is the result of comparing carriers and modulation signal. Based on the desired level at the output, the corresponding switching state can be selected from Table I and then applied to the power switches. If there is no control over the currents that flow into/out from the flying capacitors to charge/discharge the capacitors, therefore the voltage of the flying capacitors may deviate from their desired values.

The voltage deviation of the flying capacitors can be expressed as:

$$\Delta V_{cxi} = V_{cxi}.V_{cxi,ref}, x = a,b,c \text{ and } i = 1,2,3 \quad (1)$$

where VCxi are the capacitor voltages, Vcxi, ref are the nominal values which V cxi, ref = Vdc / 4 for i =1,2 and Vcx3, ref = 3Vdc / 4. To achieve capacitor voltage balancing, the deviation ΔVCxi should be close to zero.

TABLE I
Switching States Of The Proposed Five-Level Converter And Contribution Of The Ac-Side Currents To The Flying Capacitor Voltages

State	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{Cx1}		V_{Cx2}		V_{Cx3}		V_{ax}	Level
									$i_x>0$	$i_x<0$	$i_x>0$	$i_x<0$	$i_x>0$	$i_x<0$		
E	1	1	1	1	0	0	0	0	-	-	-	-	-	-	$V_{dc}/2$	4
D3	1	1	0	1	1	0	0	0	C	D	-	-	-	-	$V_{dc}/4$	3
D2	0	1	1	1	0	0	0	1	-	-	-	-	D	C		
D1	1	0	1	1	0	0	1	0	D	C	D	C	C	D		
C4	1	1	0	0	1	1	0	0	C	D	C	D	-	-	0	2
C3	1	0	0	1	1	0	1	0	-	-	D	C	C	D		
C2	0	1	0	1	1	0	0	1	C	D	-	-	D	C		
C1	0	0	1	1	0	0	1	1	D	C	D	C	-	-		
B3	0	0	0	1	1	0	1	1	-	-	D	C	-	-	$-V_{dc}/4$	1
B2	1	0	0	0	1	1	1	0	-	-	-	-	C	D		
B1	0	1	0	0	1	1	0	1	C	D	C	D	D	C		
A	0	0	0	0	1	1	1	1	-	-	-	-	-	-	$-V_{dc}/2$	0

C: Charging D: Discharging

As can be seen from the Table I, there are enough redundancy at level 1, 2 and 3 to charge and discharge the flying capacitors[8]. Level 1 is a good candidate to control voltages of capacitor Cx3 and Cx2 while Level 3 is a good candidate to control voltage of capacitors Cx3 and Cx1.

Table II shows that which switching state should be chosen in different conditions to control voltage of flying capacitors. For example, if the level is 2 and the deviation of capacitor Cx1 is more than other capacitors ((|ΔVCX1| > |ΔVCX3|) & (|ΔVCX1| > |ΔVCX2|)), it means that the main priority should be given to charge or discharge capacitor Cx1. Assume that ix> 0, if ΔVcx1 > 0, therefore the capacitor Cx1 should be discharged and thus the State C1 should be selected.

According to Table I and II, the procedure bellow should be followed to control the flying capacitor voltages:

1- The desired output level should be determined by comparing carriers and modulation signal, as shown in Fig. 2,

2- The direction of the phase current and voltages of the flying capacitors should be measured and then the capacitor voltage deviation can be determined based on (1),

and finally the appropriate switching state can be selected from Table II and the corresponding gating signals will be applied to the power semiconductors. First, the modulating signal for phase x (x=a,b,c) is compared to carriers (four carriers) and then the desired output levels are determined. If the desired output level (L) is 0 or 4, the corresponding switching state will be State A or E from Table I respectively. Otherwise, the capacitor voltages (VCX1, VCX2 and VCX3) and phase current should be measured and then based on the output level (L) the appropriate switching state should be selected from Table II

TABLE II
THE PROPOSED VOLTAGE BALANCING METHOD FOR EACH PHASE OF THE FIVE-LEVEL INVERTER

Output Level	Condition	i_x	ΔV_{CX1}	ΔV_{CX2}	ΔV_{CX3}	State
3	$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX3}\rvert$	≥0	≥0	-	-	D1
			<0	-	-	D3
		<0	≥0	-	-	D3
			<0	-	-	D1
	$\lvert\Delta V_{CX3}\rvert > \lvert\Delta V_{CX1}\rvert$	≥0	-	-	≥0	D2
			-	-	<0	D1
		<0	-	-	≥0	D1
			-	-	<0	D2
2	$\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX3}\rvert$ & $\lvert\Delta V_{CX1}\rvert > \lvert\Delta V_{CX2}\rvert$	≥0	≥0	-	-	C1
			<0	-	-	C2 / C4
		<0	≥0	-	-	C2 / C4
			<0	-	-	C1
	$\lvert\Delta V_{CX2}\rvert > \lvert\Delta V_{CX1}\rvert$ & $\lvert\Delta V_{CX2}\rvert > \lvert\Delta V_{CX3}\rvert$	≥0	-	≥0	-	C3 / C1
			-	<0	-	C2
		<0	-	≥0	-	C2
			-	<0	-	C3 / C1
	$\lvert\Delta V_{CX3}\rvert > \lvert\Delta V_{CX1}\rvert$ & $\lvert\Delta V_{CX3}\rvert > \lvert\Delta V_{CX2}\rvert$	≥0	-	-	≥0	C2
			-	-	<0	C3
		<0	-	-	≥0	C3
			-	-	<0	C2
1	$\lvert\Delta V_{CX2}\rvert > \lvert\Delta V_{CX3}\rvert$	≥0	-	≥0	-	B3
			-	<0	-	B1
		<0	-	≥0	-	B1
			-	<0	-	B3
	$\lvert\Delta V_{CX3}\rvert > \lvert\Delta V_{CX2}\rvert$	≥0	-	-	≥0	B1
			-	-	<0	B2
		<0	-	-	≥0	B2
			-	-	<0	B1

The flowchart shown in Fig.3 illustrates the procedure to control voltage of flying capacitors in each phase.

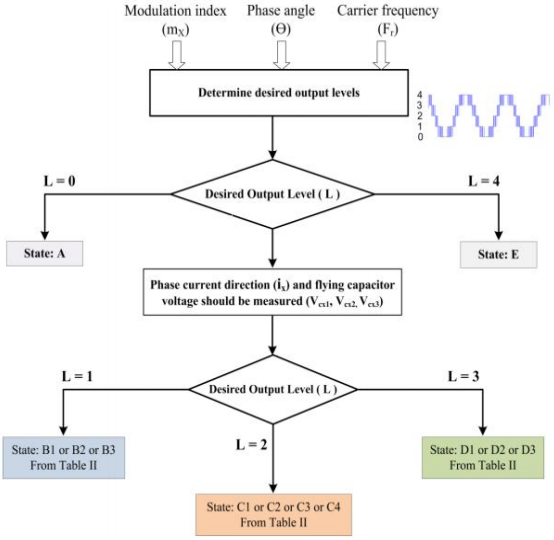

Fig.3. The procedure to control of flying capacitor voltages.

The parameters of the system are shown in Table III. The simulation also demonstrates the effectiveness of the developed SPWM to generate output voltages and to regulate and balance the voltage of flying capacitors.

TABLE III:
PARAMETERS OF THE STUDY SYSTEM
(SIMULATION)

Converter Parameters	Values	Values (p.u)
Converter Rating	5 MVA	1.0
Output Voltage	7.2 kV	1.0
Flying Capacitors	1000 µF	4.0
Input DC Voltage	12 kV	-
Output Frequency	60 Hz	1.0
Output Inductance	5.0mH	0.1
Device Switching Frequency	500 Hz	

This procedure can be applied to each leg separately to control its flying capacitor voltages, the only difference is that modulating signals should have ±120° phase shift respect to each other.

ARTIFICIAL NEURAL NETWORKS (ANN)

The ANNs are difficult to describe with a simple definition. Maybe the closest description would be a comparison with a black box having multiple inputs and multiple outputs which operates using a large number of mostly parallel connected simple arithmetic units. The most important thing to remember about all ANN methods is that they work best if they are dealing with non-linear dependence between the inputs and outputs.

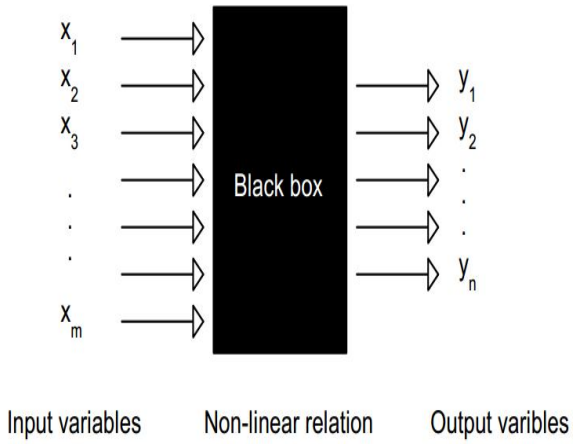

Fig.4 Neural network as a black-box featuring the non-linear relationship

ANNs can be employed to describe or to find linear relationship as well, but the final result might often be worse than that if using another simpler standard statistical techniques. Due to the fact that at the beginning of experiments we often do not know whether the responses are related to the inputs in a linear on in a nonlinear way, a good advice is to try always some standard statistical technique for interpreting the data parallel to the use of ANNs.

Basic concepts of ANNs

Artificial neuron is supposed to mimic the action of a biological neuron, i.e., to accept many different signals, xi, from many neighboring neurons and to process them in a pre-defined simple way. Depending on the outcome of this processing, the neuron j decides either to fire an output signal yj or not. The output signal (if it is triggered) can be either 0 or 1, or can have any real value between 0 and 1 (Fig. 11) depending on whether we are dealing with 'binary' or with 'real valued' artificial neurons, respectively.

Mainly from the historical point of view the function which calculates the output from the m-dimensional input vector X, f(X), is regarded as being composed of two parts. The first part evaluates the so called 'net input', Net, while the second one 'transfers' the net input Net in a non-linear manner to the output value y.

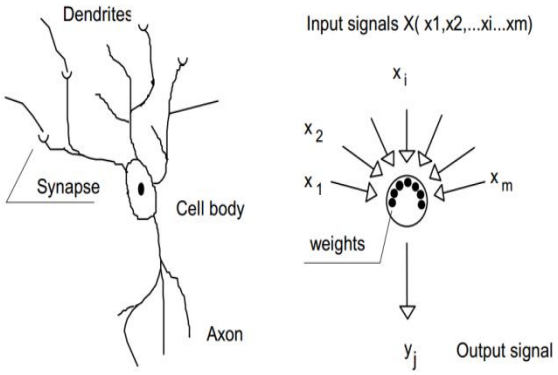

Fig. 5 Comparison between the biological and artificial neuron.

The weights wji in the artificial neurons are the analogues to the real neural synapse strengths between the axons firing the signals and the dendrites receiving those signals (Figure 5). Each synapse strength between an axon and a dendrite (and, therefore, each weight) decides what proportion of the incoming signal is transmitted into the neurons body.

Some possible forms for the transfer function are plotted in Figure 6. It is important to understand that the form of the transfer function, once it is chosen, is used for all neurons in the network, regardless of where they are placed or how

they are connected with other neurons. What changes during the learning or training is not the function, but the weights and the function parameters that control the position of the threshold value, qj , and the slope of the transfer function aj.(eqs. /2/, /3/).

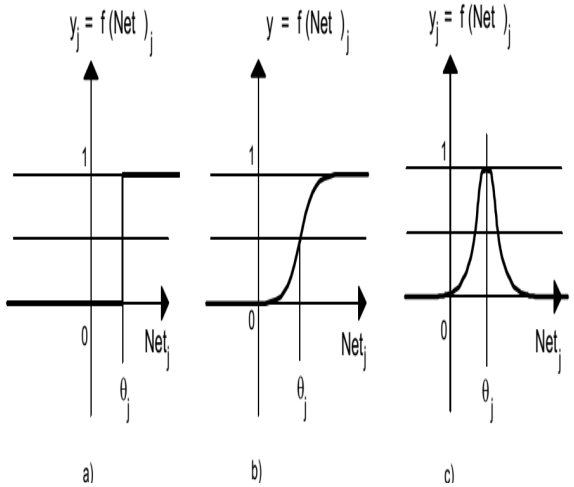

Fig. 6 Three different transfer functions: a threshold (a) a sigmoidal (b) a radial function (c) The parameter qj in all three functions decides the Netj value

Artificial neural networks (ANNs) can be composed of different number of neurons. In chemical applications, the sizes of ANNs, i.e., the number of neurons, are ranging from tens of thousands to only as little as less than ten (1-3). The neurons in ANNs can be all put into one layer or two, three or even more layers of neurons can be formed. Figure 8 show us the difference between the one and multilayer ANN structure.

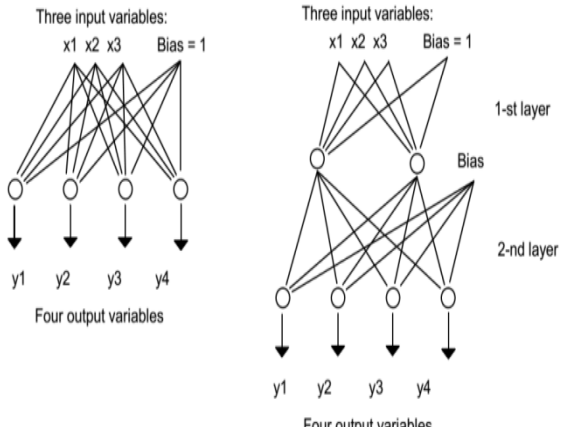

Fig. 7 One-layer (left) and two-layer (right) ANNs.

In Figure 8 the one-layer network has four neurons (sometimes called nodes), each having four weights. Altogether there are 16 weights in this one-layer ANN. Each of four neurons accept all input signals plus the additional input from the bias which is always equal to one. The fact, that the input is equal to 1, however, does not prevent the weights leading from the bias towards the nodes to be changed! The two-layer ANN (Fig. 8,right) has six neurons (nodes): two in the first layer and four in the second or output layer. Again, all neurons in one layer obtain all signals that are coming from the layer above. The two-layer network has (4 x 2) + (3x 4) = 20 weights: 8 in the first and 12 in the second layer. It is understood that the input signals are normalized between 0 and 1

SIMULATION RESULTS

The performance of the proposed five-level converter and SPWM controller has been studied during both steady-state and transient-state conditions.

A.Steady-State Analysis

Figs. 8 and 9 show the performance of the proposed converter using developed SPWM technique with different modulation indexes.

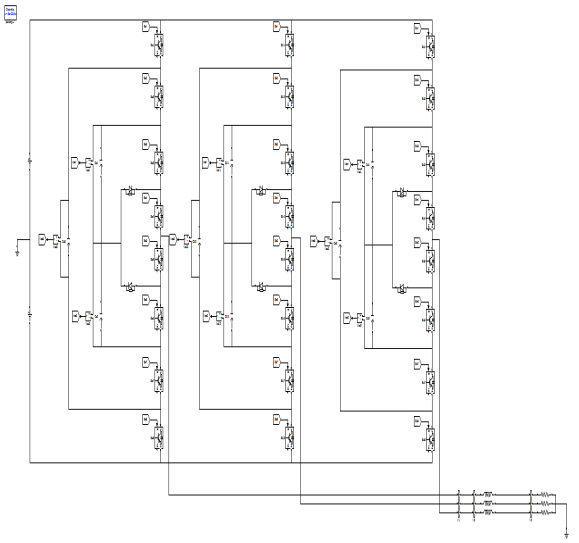

Fig.8 Block diagram of simulation.

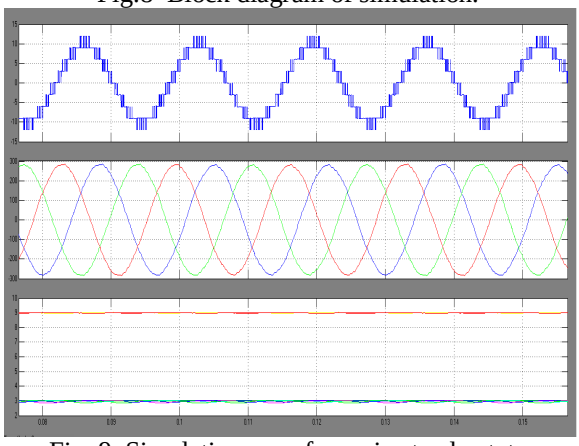

Fig. 9. Simulation waveforms in steady-state condition (a) inverter voltage, (b) output currents, and (c) voltages of flying capacitors (m=0.95).

Fig. 9 shows the inverter output voltage, output currents and flying capacitor voltages where modulation index m = 0.95 and Fig. 9 also shows the inverter output voltage, output currents and flying capacitor voltages where modulation index m = 0.65.

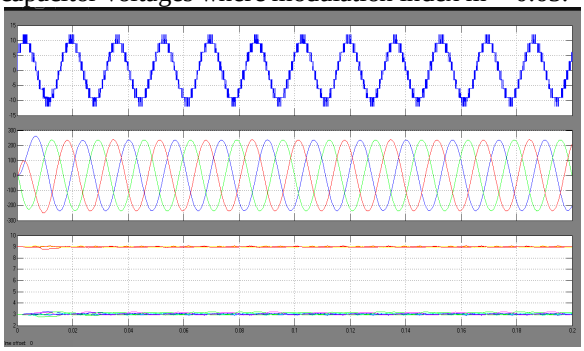

Fig. 10. Simulation waveforms in steady-state condition (a) inverter voltage, (b) output currents, and (c) voltages of flying capacitors (m=0.65).

Figs. 11 and 12 show the performance of the proposed converter where the load is inductive with PF=0.7 and capacitive with PF=-0.7 respectively.

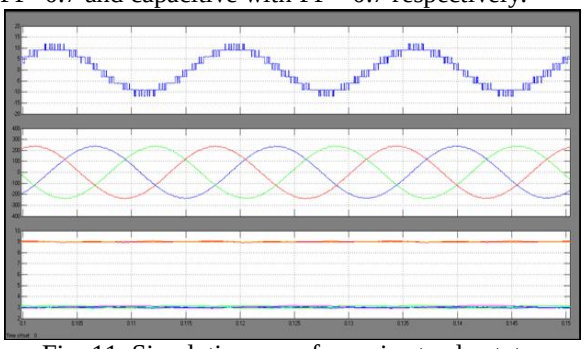

Fig. 11. Simulation waveforms in steady-state condition (inductive load) (a)inverter voltage, (b)output currents, and (c)voltages of flying capacitors (m=0.95, PF=0.7).

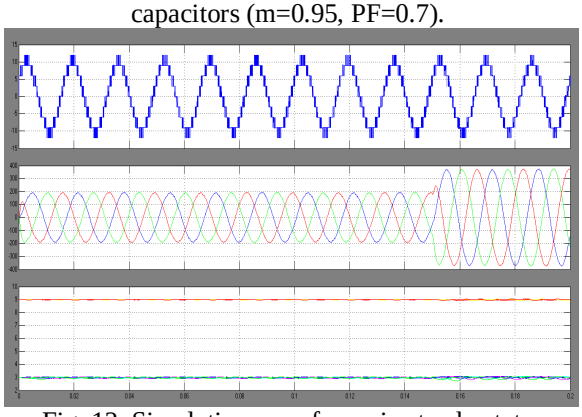

Fig. 12. Simulation waveforms in steady-state condition (capacitive load) (a)inverter voltage, (b)output currents, and (c)voltages of flying capacitors (m=0.9, PF=-0.7).

As can be seen from the Figs. 8 to 11, the proposed converter using SPWM can regulate and balance capacitor voltages under different conditions. It should be noted that the voltage stress for all the power switches are the same and equal to one-fourth of the dc-link voltage which in this case is 3000V.

B.Transient-State Analysis

In this case, step change from half-load to full-load at t = 0.15 sec has been applied to the power converter where m=0.95. As observed from Fig. 13, voltages of flying capacitors are maintained at their nominal values. The nominal value for Cx1 and Cx2 is 1/4Vdc and that is 3/4Vdc for Cx3.

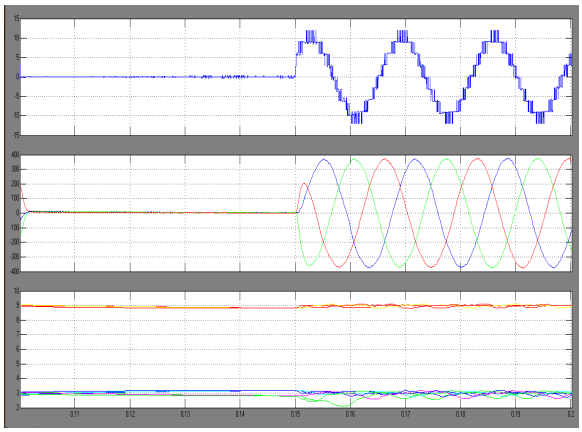

Fig. 13. Simulation waveforms in transient-state condition; load changes from half-load to full-load (a) inverter voltage, (b) output currents, and (c) voltages of flying capacitors (m=0.95).

C.Evaluation of Control Performance .

To show the performance of the controller, assume that the proposed converter is operating in normal condition and suddenly at t=0.1sec, the SPWM controller has been deactivated and at t=0.15sec the controller reactivated again.

As can be seen from Fig. 15, when the controller is deactivated the voltage of the capacitors deviate from the nominal values and when the controller reactivates the capacitor voltages start converging to their nominal values. This study shows the performance of the controller given by Table II.

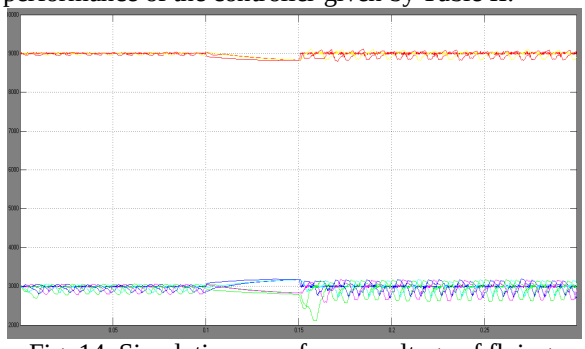

Fig. 14. Simulation waveforms; voltage of flying capacitors with and without the controller.

V. CONCLUSION

A new five-level voltage source inverter with sinusoidal pulse width modulator for medium-

voltage applications is proposed in this paper. The proposed topology is the upgrade of the four-level NNPC converter that can operate over a wide range of input voltage without any power semiconductor in series. Compared with classic multilevel converters the proposed converter has fewer components as and the voltage across the power semiconductors is only one-fourth of the dc-link. A SPWM strategy is developed to control the output voltage and regulate the voltage of the flying capacitors. The performance of the proposed converter is confirmed and the feasibility of the proposed converter is evaluated by using the simulation results.

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