VLSI Design For Convolutive Blind Source Separation

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ABSTRACT

This will exhibits a proficient Very Large Scale Integration (VLSI) plan for Convolutive Blind Source Separation (CBSS). Data boost (Infomax) approach is embraced for CBSS organize. CBSS chip configuration for the most part incorporates Infomax sifting modules and scaling factor calculation modules. In an Infomax sifting module, separating of information tests are finished by Infomax channel with the weights refreshed by Infomax driven stochastic learning rules. Furthermore, to scale factor calculation module all operations are actualized by the circuit configuration in view of a piecewise-direct estimation conspire. An effective and elite and less deferred dazzle source division method is depicted .

Key Words- Convolutive Blind Source Separation (CBSS), Infomax, Scaling factor.

1. Introduction

Blind source separation is a kind of a filtering process used to separate different sources from the mixed signals in which most of the information about sources and mixed signals is not known. This restriction makes the blind source separation a challenging task. Blind source separation becomes a very important research topics in a lot of fields such as audio signal processing, biomedical signal processing, communication systems and image processing. Simple version of mixing process is one in which without filtering effect instantaneous mixing occurs. Convolutive mixing process should be done for the audio source passing through a filtering environment before arriving at the microphones and in order to recover the original audio source convoluted blind source separation should be done. One of the conventional methods is Independent component analysis (ICA) which is used to solve the CBSS problem. Major drawback of software implementation using this technique is often highly computational intensive and more time consuming process. Providing hardware solutions for ICA-based blind source separation has drawn considerable attention because of the hardware solution achieves optimal parallelism. An analog BSS chip can be designed using above-and–sub threshold CMOS circuit techniques which integrates an i/o interface of analog, weight coefficients and adoption blocks.

Convolutive Blind Source Separation (CBSS):

During the past decades, much attention has been given to the separation of mixed sources, in particular for the blind

case where both the sources and\ the mixing process are unknown and only recordings of the mixtures are available. In several situations it is desirable to recover all sources from the recorded mixtures, or at least to segregate a particular source. Furthermore, it may be useful to identify the mixing process itself to reveal information about the physical mixing system. In some simple mixing models each recording consists of a sum of differently weighted source signals. However, in many real-world applications, such as in acoustics, the mixing process is more complex. In such systems, the mixtures are weighted and delayed, and each source contributes to the sum with multiple delays corresponding to the multiple paths by which an acoustic signal propagates to a microphone. Such filtered sums of different sources are called convolutive mixtures.

Infomax:

Infomax is an optimization principle for artificial neural networks and other information processing systems. It prescribes that a function that maps a set of input values I to a set of output values O should be chosen or learned so as to maximize the average Shannon mutual information between I and O, subject to a set of specified constraints and/or noise processes. Infomax algorithms are learning algorithms that perform this optimization process. The principle was described by Linsker in 1988.[1]

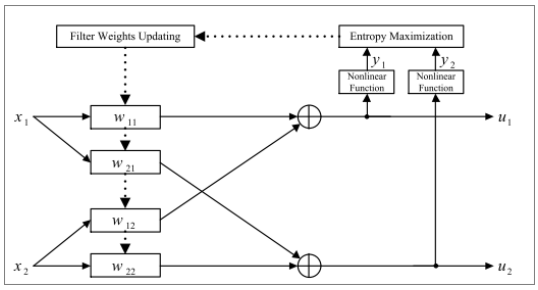


Fig. 1. Infomax-based CBSS separation network for the two-source and two sensor case.

2. Literature survey:

Jia-Ching Wang, Chien-Yao Wang, Tzu-Chiang Tai presented an efficient very-large-scale integration architecture design for convolutive blind source separation (CBSS). The CBSS separation network derived from the information maximization (Infomax) approach is adopted. The proposed CBSS chip design consists mainly of Infomax filtering modules and scaling factor computation modules. In an Infomax filtering module, input samples are filtered by an Infomax filter with the weights updated by Infomax-driven stochastic learning rules. As for the scaling factor computation module, all operations including logistic sigmoid are integrated and implemented by the circuit design based on a piecewise-linear approximation scheme. The proposed prototype chip is implemented via a semi-custom design using 90-nm CMOS technology on a die size of approximately 0.54×0.54 mm^2.

3.PROPOSED VLSI BLIND SOURCE SEPARATOR

The proposed CBSS system is shown in the FIG.2. The CBSS chip mainly consists of two functional cores: Infomax filtering module and scaling factor

computation module. Additionally, the Infomax filtering outputs are added with the help of two small carry-save adders (CSAs). The current prototype chip is used for two sources and two sensors by utilizing four Infomax filtering modules along with two scaling factor computation modules.

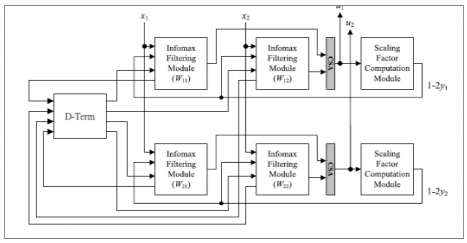


FIG.2 : The block diagram of a proposed CBSS system.

4. INFOMAX FILTERING MODULE

The Infomax filtering module for the proposed system is shown in fig.3. In the fig. 1, the CBSS separation network contains four causal FIR filters. These filters are adaptive because stochastic learning rules which are derived from the Infomax approach will alter the tap coefficients and are thus referred to herein as the Infomax adaptive filter or the Infomax filter. The Infomax filtering module is exemplified with six taps. In the Infomax filtering module, an input sample passes through lower and upper register chains. These samples are multiplied with filter weights and scaling factors, respectively. The multiplication results of all of the taps are accumulated by a two-stage summation. The first stage adopts carry lookahead adders to generate the intermediate addition results for multiplication of every two successive taps. The above intermediate addition results are summed up by using a carry save addition scheme. A CSA(carry save adder) can accept more than two data inputs.

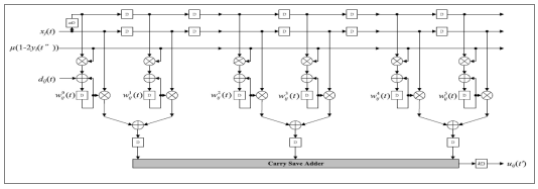


FIG.3: Infomax filtering module.

4. SCALING FACTOR COMPUTATION MODULE

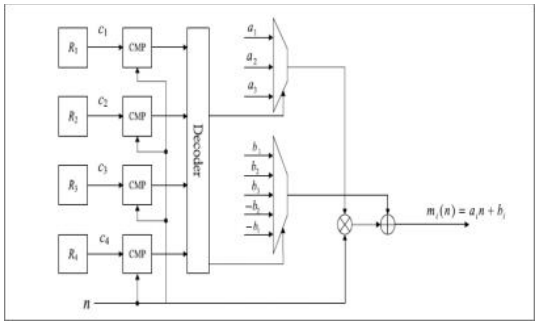
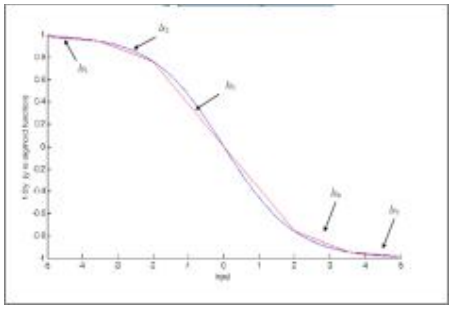


FIG.4:Scaling Factor Computation Module

Fig.4 describes the proposed circuit for the scaling factor computation module. The linear equation evaluation with input ui(t) and ai and bi are equation parameters and are implemented using a multiplier and an adder. In order to choose corresponding ai and bi, a line segment has to be selected by two multipliers. The scaling factor is calculated by using the formula s(t) = 1 − 2y(t), where y(t) = (1+e -u(t)) -1. If y(t) is known, −2y(t) can be generated first using 2's complement and a left shift to y(t). The scaling factor s(t) is then obtained by adding −2y(t) and one. The above procedure is simple. The scaling factor commutation is approximated directly rather than performing logistic sigmoid computation first and then calculating 1 − 2y(t). The target function to be

approximated by linear piecewise scheme is

S(t) = 1-2/(1 + e u i (t)) Where, s(t) = scaling factor.



. FIG.5 : Five line segment approximation to the scaling factor computation.

According to our numerical analysis, five line segments are sufficient to approximate with a negligible error. Let lsi, i = 1, 2, . . , 5 denote the ith line segment, and ci represent the connected point between two consecutive line segments. To implement the line-segment approximation, the circuit design for scaling factor computation is to calculate single variable linear equations. For the equation of lsi which corresponding to mi(n) = ai n + bi, i = 1, 2, . . . , 5, where n = ui(t). As the slopes of ls1 and ls5 are the same, these two line segments share the equation parameters a1. In the same manner, line segments ls2 and ls4 share the equation parameters a2. Furthermore, according to the symmetry in Fig. 5, the bias used for line segment ls5, e.g., −b1, is the negative of the bias b1 used for line segment ls1. In addition, line segments ls4 and ls2 use biases −b2 and b2, respectively .As for the d0 ij(t) , this study designs a Dterm unit to execute dij(t) = cofactor(wij)(detW0) -1. The architecture of the D-term unit is shown in Fig. 6. The Dterm unit consists of a determinant circuit to find

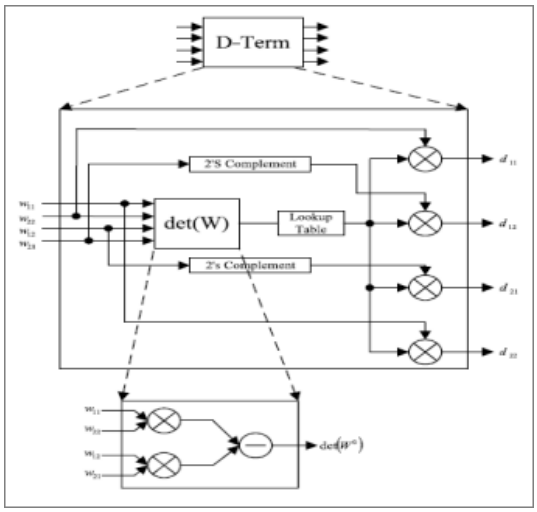


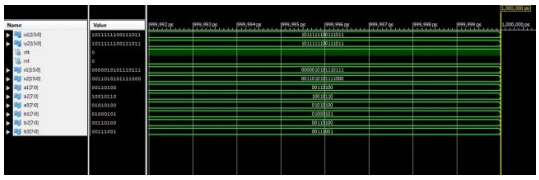
FIG.6: Architecture of a D-term unit.

Or to obtain the detW0 and in order to generate the inverse of detW0, lookup table is used. Since W is a 2 × 2 matrix, the cofactors(wij) are w22, −w21, −w12, and w11, which are multiplied by (detW0) -1 in parallel using four multipliers.

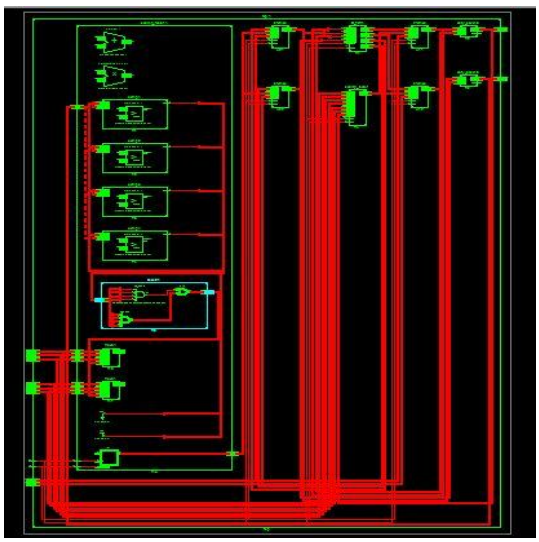
Conclusion:

An efficient VLSI architecture design for CBSS with less delay has been presented in this paper. The architecture mainly consists of Infomax filtering modules and scaling factor computation modules and a D-term. CBSS separation network derived from the Infomax approach. The proposed system has high performance and has less delay as compared with the other existing system. By the usage multiplier in Infomax filter increases the speed as well as performance of the proposed system.

Simulation Results:



RTL Schematic



Design Summary

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	256	93120	0%
Number of Slice LUTs	288	46560	0%
Number of fully used LUT-FF pairs	74	470	15%
Number of bonded IOBs	82	240	34%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	56	288	19%

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