MODELING AND SIMULATION OF NESTED NEUTRAL POINT CLAMPED (NNPC) INVERTER BY USING A CAPACITOR VOLTAGE-BALANCING METHOD

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ABSTRACT-A capacitor voltage-balancing method for a nested neutral point clamped (NNPC) inverter is proposed in this paper. To control and balance flying capacitor voltages the proposed capacitor voltage-balancing method takes advantage of redundancy in phase switching states. The proposed method needs very few computations and also easy to implement. The NNPC inverter is a newly developed four-level voltage source inverter for medium-voltage applications. The NNPC topology has two flying capacitors in each leg. In order to ensure that the inverter can operate normally and all switching devices share identical voltage stress, the voltage across each capacitor should be controlled and maintained at one-third of dc bus voltage. The proposed method is easy to integrate with different pulse width modulation schemes. By using the simulation results we can analyze the effectiveness and feasibility of the proposed method.

INTRODUCTION

Nowadays, Multilevel inverters are very popular in medium voltage applications and motor drives due to reduction of harmonics, low voltage stress on switches, low switching frequency, and less switching losses [1]. The multilevel inverters categorized into neutral point clamped (NPC) inverter, flying capacitor (FC) inverter, cascaded H-bridge inverter, and modular multilevel converter [2]–[3].

Several control techniques and modulation strategies including capacitor voltage-balancing methods have been developed in the literature for multilevel inverters [4]. In this paper a new multilevel topology is proposed. i.e, nested neutral point clamped (NNPC) inverter shown in Fig. 1.

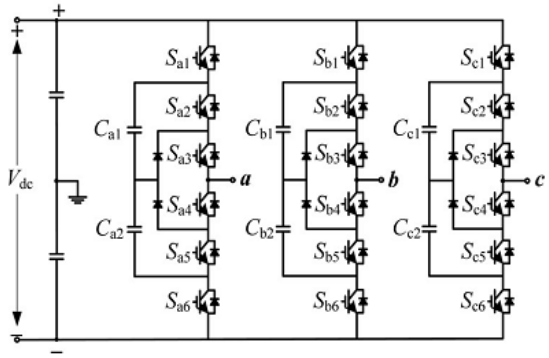


Fig. 1. Three phase nested neutral-point clamped (NNPC) inverter.

This topology is a combination of an FC topology with an NPC topology, which provides four levels in output voltage. In comparison with the four-level NPC inverter, the NNPC inverter has less number of diodes, and in comparison to four-level FC inverter, it has fewer capacitors [6]. All switches in the topology have the same voltage stress equal to one-third of dc-link voltage. The NNPC inverter can operate in a wide range of 2.4– 7.2 kV without the need for connecting power devices in series. As can be seen from Fig. 1, the NNPC topology has two FCs in each leg. The voltage across each capacitor should be controlled and balanced at one-third of dc-link voltage (Vdc/3) to ensure that the inverter can operate normally [6].

In order to mitigate the aforementioned drawbacks, a new capacitor voltage-balancing method for the NNPC inverter is proposed in this paper. In the proposed method, simple logic tables are developed to control the voltages of FCs. The proposed method has the following features:

1) The method is suitable for and can be easily integrated with different pulse width modulation (PWM) schemes such as SPWM and SVM, etc;

2) The method uses simple logic tables, needs very few computations, and is easy to implement. The difference in the topology causes different behavior in capacitor voltages and thus need different voltage-balancing methods.

In order to control output voltage and get FC voltage balance, a space vector modulation (SVM) technique is presented in [6] for NNPC inverter. In this method, a cost function is defined based on the energy stored in capacitors. The cost function needs to be calculated repeatedly for each redundant switching state in every sampling period to find the best switching state to balance FC voltages.

OPERATION OF THE NNPC INVERTER AND BEHAVIOR ANALYSIS OF THE CAPACITOR VOLTAGES

A. Operation of the NNPC Inverter

The three-phase NNPC inverter is shown in Fig. 1. Each phase of the inverter consists of six switches, two clamping diodes, and two FCs. The

voltages of the FCs should be kept at one-third of dc bus voltage (Vdc/3) to generate four output levels in phase voltage and ensure that all the power switches share the same voltage stress. Table I shows the phase voltagevk (k=a, b, c), output levelLk, as well as the corresponding phase switching stateSk. For each phase, the four distinct output voltages are −Vdc/2, −Vdc/6, Vdc/6, and Vdc/2, corresponding to the four output levels 0, 1, 2, and 3, respectively. The relationship of vk and Lk can be expressed as

$$v_k = (2L_k - 3)V_{dc}/6 \qquad (1)$$

As can be seen from Table I, levels 0 and 3 have no redundant switching state, while levels 1 and 2 both have two redundant switching states. The redundant switching states for level 1 are 1A[001101] and 1B[100110]. The two redundant switching states generate the same output voltage−Vdc/6with different switches ON and OFF. For level 2, the two redundant switching states are 2A[011001]and 2B[101100], generating the same phase voltage Vdc/6 with different switches ON and OFF.

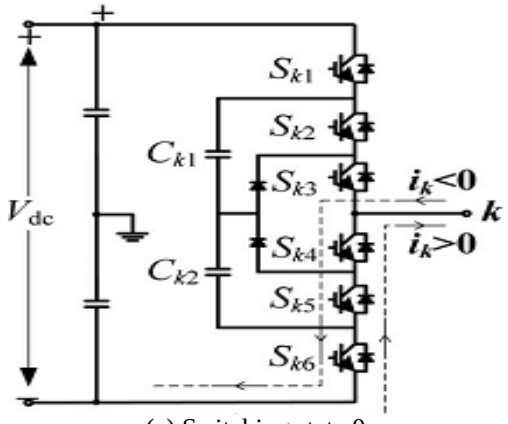
TABLE I: PHASE VOLTAGES AND SWITCHING STATES IN NNPC INVERTER (k=a, b, c)

Phase voltage,v_k	**Output Level,L_k**	**Phase switching States s_k**	**Switching states of each device**					
			s_{k1}	s_{k2}	s_{k3}	s_{k4}	s_{k5}	s_{k6}
$V_{dc}/2$	3	3	1	1	1	0	0	0
$V_{dc}/6$	2	2A	0	1	1	0	0	1
		2B	1	0	1	1	0	0
$-V_{dc}/6$	1	1A	0	0	1	1	0	1
		1B	1	0	0	1	1	0
$-V_{dc}/2$	0	0	0	0	0	1	1	1

B. Behavior Analysis of the Capacitor Voltages in the NNPC Inverter

Different redundant switching states have different impacts on FC voltages. The analysis of this impact is illustrated in Fig. 2, in which the six overall switching states are analyzed.

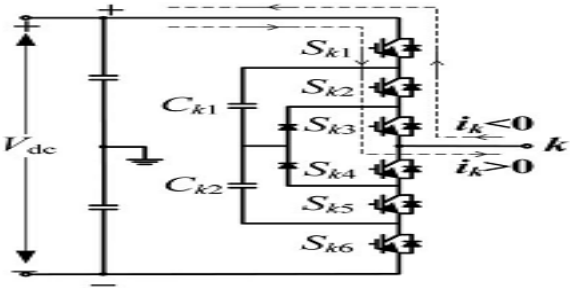
In Fig. 2, Ck1 andCk2 are the two series FCs in the phase k(k=a, b, c), whose voltages are denoted byVCk1 andVCk2. The behavior of the capacitor voltages depends on the switching state Sk and the phase current ik.



(a) Switching state 0.

Fig. 2. Impacts of different phase switching states and phase current on capacitor voltages in NNPC inverter

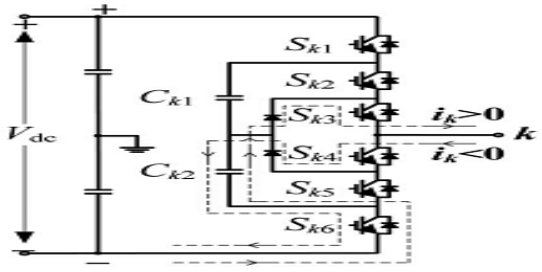
As shown in Fig. 2(a) and (f), the switching states 0 and 3 (corresponding to levels 0 and 3, respectively) have no impact on the capacitor voltages due to the fact that no current flows through the capacitors.



(f) Switching state 3

Fig. 2. Impacts of different phase switching states and phase current on capacitor voltages in NNPC inverter

Levels 1 and 2 always have impacts on capacitor voltages. The impacts are different for different redundant switching states and also depend on the direction of phase current.

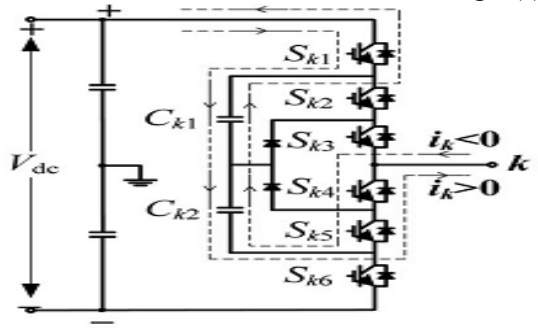


(b) Switching state 1A

Fig. 2. Impacts of different phase switching states and phase current on capacitor voltages in NNPC inverter

For level 1, if the redundant switching state 1A is employed and ik >0, the capacitorCk2discharges andVCk2 decreases, and if ik <0, the capacitor Ck2 charges andVCk2 increases, while there is no impact on capacitorCk1,asshown in Fig. 2(b).

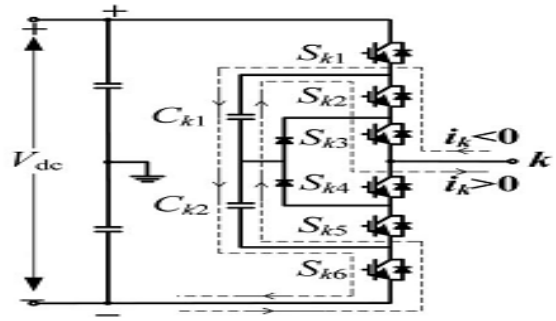
If the redundant switching state 1B is employed, both the capacitorCk1 andCk2 charge and capacitor voltage VCk1 andVCk2 increase when ik >0, and both Ck1 andCk2 discharge andVCk1 andVCk2 decrease when ik <0,as shown in Fig. 2(c).



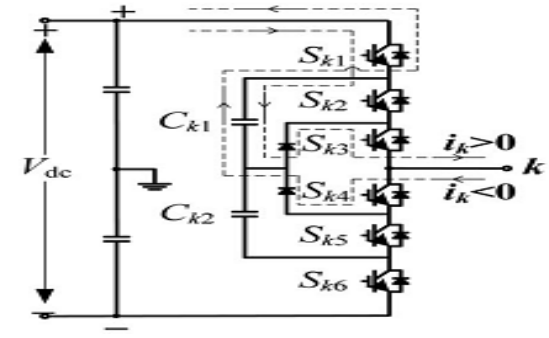
(c) Switching state 1B

Fig. 2. Impacts of different phase switching states and phase current on capacitor voltages in NNPC inverter

A similar analysis can be applied to level 2 as shown in Fig. 2(d) and (e) for the redundant switching states 2A and 2B.



(d) Switching state 2A



(e) Switching state 2B

Fig. 2. Impacts of different phase switching states and phase current on capacitor voltages in NNPC inverter.

Table II summarizes the behaviors of FC voltages under different switching states and phase currents. As analyzed above, levels 0 and 3 have no impact onVCk1 andVCk2, while level 1 (with redundant switching state 1A and 1B) and level 2 (with redundant switching state 2A and 2B) have different impacts on VCk1 andVCk2 depending on the selected switching state and the direction of phase current.

PROPOSED CAPACITOR VOLTAGE-BALANCING METHOD

A. Algorithm of the Proposed Method

If there is no control on the voltages of the FCs in the NNPC converter, the FC voltages will deviate from their desired value, and this is because there is no control over the currents that flow into/out from the capacitors. The difference between the actual FC voltage and the desired value (Vdc/3) can be defined as voltage deviation of the FC and can be expressed as

$$\Delta V_{Cki} = V_{Cki} - V_{dc}/3 \qquad (2)$$

Where VCki are the capacitor voltages and ΔVCki are the deviations of the capacitor voltages, k=a, b, c, and i=1,2.

To achieve capacitor voltage balancing, ΔVCki should be controlled close to zero. If ΔVCki>0, the switching state that makes the capacitor voltage decrease should be selected, whereas if ΔVCki<0, the switching state that makes the capacitor voltage increase should be selected. However, there is a difficulty in implementing the above principle since the two capacitors in an inverter leg are coupled (charged/discharged jointly) as shown in Table II.

TABLE II: BEHAVIOR OF FC VOLTAGES UNDER DIFFERENT PHASE SWITCHING STATES AND PHASE CURRENTS

Phase voltage, v_k	Output level, L_k	Phase current, i_k	The behavior of flying capacitor voltages V_{Ck1}	V_{Ck2}
$V_{dc}/2$	3	-	No change	No change
$V_{dc}/6$	2	>0	Decrease (2A), Increase (2B)	Decrease (2A), No change (2B)
		<0	Increase (2A), Decrease (2B)	Increase (2A), No change (2B)
$-V_{dc}/6$	1	>0	No change (1A), Increase (1B)	Decrease (1A), Increase (1B)
		<0	No change (1A), Decrease (1B)	Increase (1A), Decrease (1B)
$-V_{dc}/2$	0	-	No change	No change

Table III shows the logic table for controlling capacitor voltageVCk1. The following cases are listed in the table:
1) If ΔVCk1 <0, the switching state 2A should be selected if ik <0; otherwise, the switching state 2B is employed if ik <0;
2) If ΔVCk1 ≥;0, the switching state 2B should be selected if ik <0; otherwise, the switching state 2A is employed if ik≥;0.

In this condition, the capacitor voltage VCk1 is completely controllable regardless of the direction of the inverter phase current.

TABLE III: LOGIC TABLE FOR BALANCING CAPACITOR VOLTAGE VCk1

Input conditions			Output Results
L_k	ΔV_{ck1}	i_k	The selected switching state(s_k) for controlling V_{ck1}
2	< 0	< 0	2A
		≥ 0	2B
	≥ 0	< 0	2B
		≤ 0	2A

Table IV shows the logic table for controlling capacitor voltageVCk2. Similar to Table III, the following cases are listed:
1) If Δ; VCk2 <0, the switching state 1A should be selected if ik <0; otherwise, the switching state 1B is employed if ik ≥;0;
2) If Δ; VCk2 ≥;0, the switching state 1B should be selected if ik <0; otherwise, the switching state 1A is employed if ik ≥;0.

In this condition, the capacitor voltage VCk2 is completely controllable regardless of the direction of the inverter phase current.

TABLE IV: LOGIC TABLE FOR BALANCING CAPACITOR VOLTAGE VCk2

Input conditions			Output Results
L_k	ΔV_{ck1}	i_k	The selected switching state(s_k) for controlling V_{ck1}
2	< 0	< 0	1A
		≥ 0	1B
	≥ 0	< 0	1B
		≤ 0	1A

The simplified tables are given in Tables V and VI. In this case, ΔVCki×ik is used as input variable and the logic is simplified into two cases for each table. ΔVCki×ik could also be replaced by sign (ΔVCki)×sign(ik)and the operator "×" could be processed with logical operation.

TABLE V: SIMPLIFIED LOGIC TABLE FOR BALANCING CAPACITOR VOLTAGE VCk1

Input conditions		Output Results
L_k	ΔV_{ck1}	The selected switching
	$*i_k$	state(s_k) for controlling V_{ck1}
2	< 0	< 0	2B
		≥ 0	2A

TABLE VI: SIMPLIFIED LOGIC TABLE FOR BALANCING CAPACITOR VOLTAGE VCk2

Input conditions		Output Results
L_k	ΔV_{ck1} $*i_k$	The selected switching state(s_k) for controlling V_{ck1}
2	< 0 < 0	1B
	≥ 0	1A

B. Integration with Different PWM Schemes

The proposed capacitor voltage-balancing method is suitable for and can be easily integrated with different PWM schemes. The schematic diagram for integration is shown in Fig. 3, which could be summarized into the following four steps:
1) First, the output voltage level Lk can be generated by different PWM schemes, such as SPWM, SVM, etc.
2) The voltage deviationΔVCk1 andΔVCk2 should be calculated by (2), and also, the direction of the phase current ik should be determined;
3) Tables V and VI are employed to determine the best redundant switching state out of 1A, 1B and 2A, 2B;
4) Finally, the gating signals are generated and applied to power semiconductors.

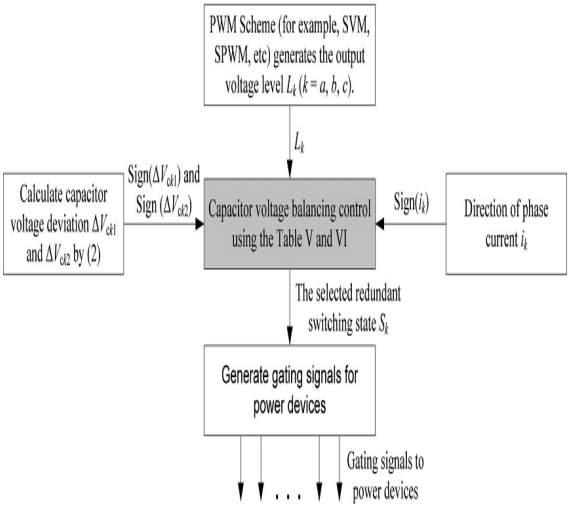


Fig. 3. Schematic diagram for integration of the proposed capacitor voltage-balancing method with PWM schemes.

This procedure indicates that the proposed capacitor voltage balancing method can be easily integrated with different modulation schemes, and it is simple and easy to implement.

SIMULATION RESULTS

To verify the proposed capacitor voltage-balancing method, simulation studies have been done by using MATLAB/ Simulink. Simulation parameters are shown in Table VII.

TABLE VII: SIMULATION PARAMETERS

Simulation parameters	values
Output Power	1MVA
Output Voltage	4160V
Flying capacitors	819μF(5.3p.u)
Switching frequency	700HZ
DC Bus voltage	5883v
Fundamental Frequency	60HZ
Load Inductance	24.42mH
Load Resistance	14.65Ω

Modulation index ma used in this paper is given by (3), in which Vref is the given peak phase voltage reference, and Vdc is dc bus voltage

$$m_a = \sqrt{3}V_{ref}/V_{dc} \qquad (3)$$

Two PWM schemes, SPWM and SVM, integrated with the proposed capacitor voltage-balancing method, have been studied in both steady state and transient state.

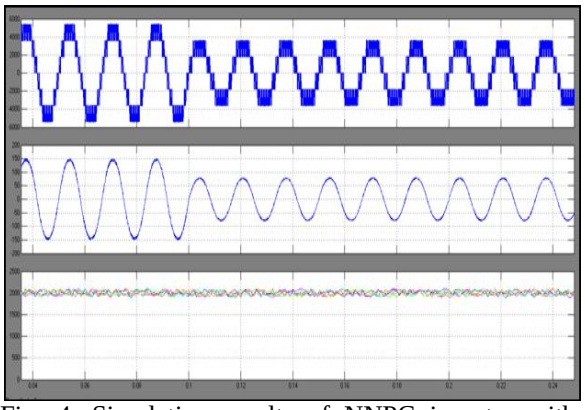


Fig. 4. Simulation results of NNPC inverter with SPWM and the voltage balancing method for ma =0.8 (t<0.1 s) and ma =0.5 (t>0.1 s). (a) Line–line voltage. (b) Phase current. (c) Six FC voltages

Fig. 4 illustrates the simulation results of the NNPC inverter with SPWM and the proposed voltage-balancing method.

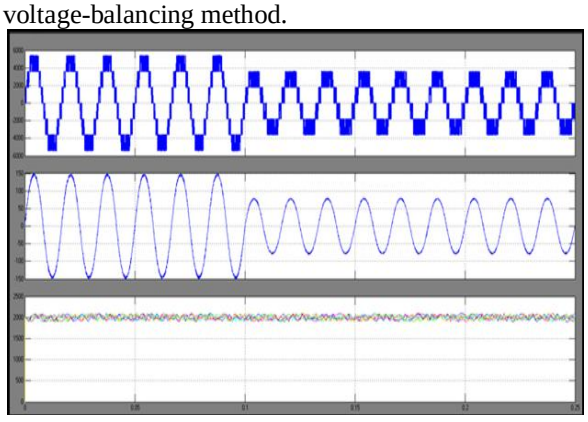


Fig. 5. Simulation results of NNPC inverter with SVM and the voltage balancing method for ma =0.8 (t<0.1 s) and ma =0.5 (t>0.1 s). (a) Line–line voltage. (b) Phase current. (c) Six FC voltages.

Fig. 5 shows the simulation results of NNPC inverter when SVM and the proposed voltage-balancing method are applied, with ma =0.8when<0.1s, and ma =0.5when>0.1s.

Dynamic processes of the FC voltages are also investigated and shown in Fig. 6 for SPWM scheme and in Fig. 7 for SVM scheme with the proposed voltage-balancing method.

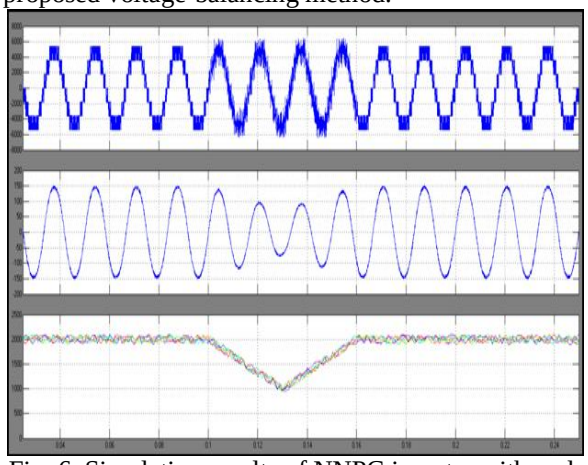


Fig. 6. Simulation results of NNPC inverter with and without the capacitor voltage-balancing control under SPWM scheme. (a) Line–line voltage. (b) Phase current. (c) Six FC voltages.

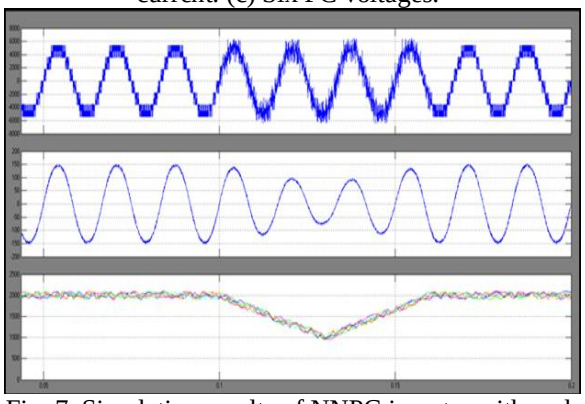
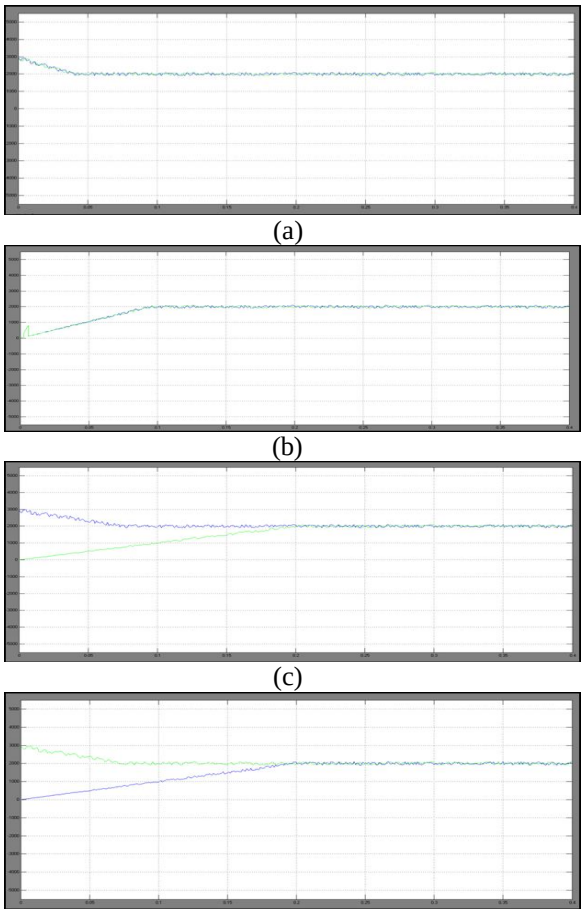


Fig. 7. Simulation results of NNPC inverter with and without the capacitor voltage-balancing control under SVM scheme. (a) Line–line voltage. (b) Phase current. (c) Six FC voltages.

Four different initial capacitor voltage unbalances have been studied to verify the ability of the voltage-balancing method. The results with ma =0.8are shown in Fig. 8.



(a)

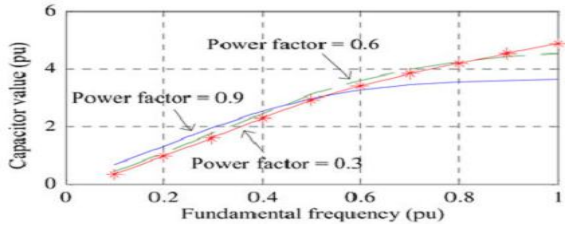
(b)

(c)

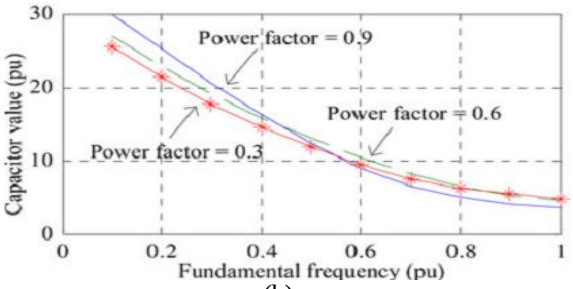
(d)

Fig. 8. Capacitor voltages ofVCa1 andVCa2 starting with different initial voltage unbalances (ma =0.8). (a)VCa1 =VCa2 =Vdc/2.(b)VCa1 = VCa2 =0.(c)VCa1 =Vdc/2andVCa2 =0.(d)VCa1 =0andVCa2 = Vdc/2.

As previously analyzed, the two capacitors in a leg of the NNPC inverter are coupled. The coupling will bring some limitations to the inverter in some applications in terms of the capacitor size.



(a)



(b)

Fig. 9. FC value versus the inverter fundamental frequency with maximum peak-to-peak capacitor voltage ripple of 15%. (a) Fan/pump type of loads. (b) Constant torque type of loads.

Under these conditions, the required capacitor sizes in per unit (p.u.) are given in Fig. 9(a) and (b) for fan/pump and constant torque types of loads, respectively.

CONCLUSION

In this paper, proposes a capacitor voltage-balancing method for a four-level NNPC inverter. At different PWM schemes the proposed method is easy to integrated. The proposed method takes advantage of redundancy in phase switching states to control and balance the FC voltages. For the control of capacitor balancing simple and effective logic tables are developed. The method is easy to implement and needs very few computations. The limitation of the NNPC inverter in terms of the voltage balancing and capacitor size is also investigated. The effectiveness and feasibility of the proposed method is determined by using the simulation results and also analyze the proposed method.

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