SWITCHING CONTROL OF BUCK CONVERTER BASED ON ENERGY CONSERVATION PRINCIPLE

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ABSTRACT: In this project we are implementing the switching control scheme (SCS) which is depend upon the energy conservation principle for buck converters. Then the content of the SCS will depend upon the conservation of energy in circuit. It will always keep the balance between the energy which is is injected into a circuit and the sum of the energy that is consumed by the load and stored in reactive components. The SCS not only regulates the output voltage of the buck converter accurately under static conditions, but also improves its dynamic responses to disturbances of input voltage and load current. Moreover both the continuous current mode and the discontinuous current mode of operation of the SCS and the stability analysis is estimated by the Lyapunov stability criterion which shown in various cases. By utilizing the simulation results we can verify the attractiveness and possibility of utilizing this method to control buck converters.

Index Terms—Buck converter, dynamic response, energy conservation principle, stability analysis, switching control.

INTRODUCTION

According to the voltage regulation criteria for digital circuit's supply voltage become more stringent, there is an increasing demand for high dynamic performance power converters. Until now, PID controllers are still one of the most commonly used control methods for converters. However, the PID control systems suffer from the limitations of slow compensator networks, which lead to poor dynamic performances of converters [1].

As control methods play an important role on improving the dynamic performance of converters, various control methods have been proposed to provide improved dynamic performances. The hysteresis control, as presented in [2]–[4], provides fast dynamic responses, since the conventional feedback compensation network is removed. However, the drawbacks of this method are its variable switching frequency and nonzero steady-state error. Sliding-mode control (SMC) is one of the effective non-linear robust control approaches, since it provides system dynamics with an invariance property to uncertainties once the system dynamics are controlled in the sliding mode [5]–[7]. However, there are some problems to be solved, such as chattering phenomena and nonconstant switching frequency, when conventional SMC is used in the power converters. While its inhibitory capability to variations of input voltage is satisfactory, the inhibitory capability to load changes is still poor. Recently, in [10]–[12], a control algorithm based on the principle of capacitor charge balance has been studied for dc–dc converters to achieve optimal dynamic performance under load current changes. However, the accurate calculation of the duty-ratio required by this control algorithm is difficult to achieve.

An ideal buck controller would behave linearly during steady-state conditions for tight voltage regulation and nonlinearly during transient conditions for fast response. It is demonstrated in that by employing two separate controllers for steady-state operation and for transient operation, the dynamic response can be improved while not sacrificing the steady-state accuracy. However, the accurate detection of the time when disturbances occur is not easy. However, the main drawback of this scheme is that it is designed based on working in DCM. Under CCM, the reference current is difficult to calculate, since not all the energy stored by the inductor is transferred to the load in one switching cycle.

DERIVATION OF THE S WITCHING CONTROLLER

The structure of a buck converter is shown in Fig. 1, where i represents the current of inductor L, io represents the current of the load R, and uo represents the output voltage. For the buck converter, the energy conservation in the circuit is expressed as follows:

$$W_{in}(n) = W_{out}(n) + \Delta W_l(n) + \Delta W_c(n) + \Delta W_s(n)$$

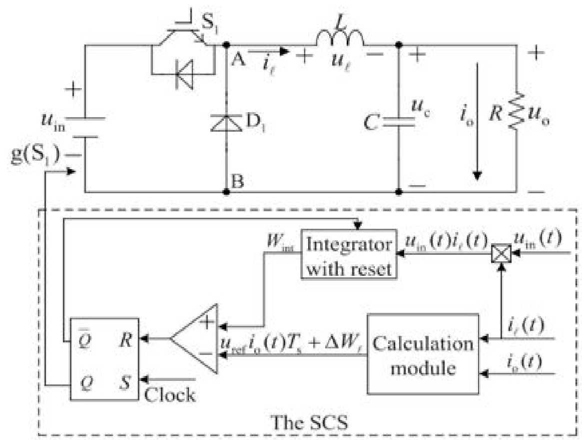

Fig :1 structure of a buck converter with the SCS

it means that, during the nth switching cycle [(n − 1)Ts, nTs), the energy that is injected into the circuit Win(n) should be equal to the sum of the output energy Wout(n), the energy that the reactive components (L and C) store (Wc(n)+ W(n)), and the conduction losses of the switch and the diode Ws(n).

The following proves that Wc(n) in (1) can be ignored. First, the output voltage uo and capacitor voltage uc are different due to the equivalent series resistance (ESR) of the capacitor, but if the ESR is negligible, then we can assume that uc is equal to uo. Then compared with the average output voltage, the output voltage ripple is negligible. And as our purpose is to ensure that uo is always equal to the reference voltage uref, which is a constant value, uo can be substituted by uref. The above assumptions give

$$U_c(t) = U_O(t) = U_{ref}$$

And the energy the capacitor stores is calculated using

$$\Delta W_c(t) = \int_{(n-1)T_s}^{t} U_c(t)i_c(t)dt \quad (t \in [(n-1)T_s, nT_s]))$$

As the capacitor C works the entire cycle during each switching cycle n, Wc(n) is calculated in

$$\Delta W_c(n) = \int_{(n-1)T_s}^{(n-1)T_s+T_s} U_c(t)i_c(t)dt$$

where ic(t) represents the capacitor current, which is calculated in

$$i_c(t) = C\frac{dU_c(t)}{dt}$$

Based on (2), Wc(n) can be obtained as

$$i_c(t) = C\frac{dU_c(t)}{dt} = C\frac{dU_{ref}}{dt} = 0 \rightarrow \Delta W_c(n) = 0$$

Thus Wc(n) in (1) can be ignored, and then the energy conservation in the circuit can be rewritten as follows:

$$W_{in}(n) = W_{out}(n) + \Delta W_l(n) + \Delta W_s(n) \; (n = 1,2 \ldots\ldots\ldots)$$

After obtaining (7), Win, Wout, Wand Ws of the buck converter working in CCM and DCM are calculated though the state analysis in the following of this section, respectively.

Continuous Conduction Mode

Under the CCM operation mode, the buck converter operates in two states:
1) state 1—switch S1 is ON and
2) state 2—S1 is OFF. Thus, during the nth switching cycle, we have

$$t_{ON}(n) + t_{OFF}(n) = T_s \qquad (n = 1,2,3,\ldots\ldots\ldots)$$

where tON(n) and tOFF(n) represent the opening and closing durations of S1 , respectively.

State 1: when S1 is ON, energy is injected into the circuit, and i flows through the loop (uin → S1 → L → C R → uin). In this switching state, L is charged, and S1 and R consume energy, and uAB is obtained using

$$u_{AB}(t) = u_{in}(t) - u_{sat} \quad (t \in [(n-1)T_s, (n-1)T_s + t_{on}(n))$$

where usat represents the ON-state voltage drop of S1 . State 2: when S1 is OFF, no energy is fed into the circuit, however, i continues flowing through the loop (D1 → L → C R → D1). In this switching state, L is discharged, and D1 and R consume energy, and uAB is obtained using

$$u_{AB}(t) = -u_d \quad (t \in [(n-1)\,T\_s + t\_on\,(n), nT_s))$$

where ud represents the ON-state voltage drop of the diode D1 .

The above state analysis shows that the voltage source works in the time interval from (n− 1)Ts to (n− 1)Ts + tON(n), while L and R work in the entire switching cycle. Thus, the values of Win(n), Wout(n), W(n), and Ws(n) during the nth switching cycle can be obtained as follows:

$$W_{in}(n) = \int_{(n-1)T_s}^{(n-1)T_s+T_{ON}(n)} U_{in}(t)i_l(t)dt$$

$$W_{out}(n) = \int_{(n-1)T_s}^{(n-1)T_s+T_s} U_0(t)i_0(t)dt$$

as uo = uref from (2), (12) becomes

$$W_{out}(n) = u_{ref}i_o(t)T_s$$

W(n) and Ws(n) are calculated as follows:

$$\Delta W_l(n) = \int_{(n-1)T_s}^{(n-1)T_s+T_s} U_l(t)i_l(t)dt$$

$$W_s(n) = \int_{(n-1)T_s}^{(n-1)T_s+t_{ON}(n)} U_{sat}i_l(t)dt + \int_{(n-1)T_s+t_{on}(n)}^{nT_s} u_d\, i_l(t)dt$$

Discontinuous Conduction Mode

Under the DCM operation mode, the buck converter operates in three states, in which switch S1 is ON for a duration of tON(n) and is OFF for durations tOFF1(n) and tOFF2(n), and tON(n) + tOFF1(n) + tOFF2 = Ts(n).

State 1: when S1 is on, energy is injected into the circuit, and i flows through the loop (uin → S1 → L → C R → uin). In this switching state, L is charged, and S1 and R consume energy, and uAB is obtained using

$$u_{AB}(t) = u_{in}(t) - u_{sat} \quad (t \in [(n-1)T_s, (n-1)T_s + t_{ON}(n)])$$

State 2: when S1 is OFF, no energy is fed into the circuit. Energy stored in L is discharged through the loop (D1 → L → C R → D1). In this switching state, L is discharged, and D1 and R consume energy. uAB is obtained in

$$u_{AB}(t) = -u_d \quad (t \in [(n-1)T_s + t_{ON}(n), (n-1)T_{s+t_{ON}(n)+t_{OFF1}(n)}])$$

State 3: when S1 is still OFF and energy stored in L is discharged out, i = 0. However, the load still consumes energy from the capacitor. In this switching state, R consumes energy, and uAB is obtained using

$$u_{AB}(t) = 0 \quad (t \in [(n-1)T_s + +t_{ON}(n) + t_{OFF1}(n), nT_s])$$

By combining state 1, state 2, and state 3, Win(n), Wout(n), W(n), and Ws(n) under DCM can be calculated similarly to that of the CCM operation mode.

Combining the aforementioned state analysis, it is observed that (16) and (20) can both be realized by controlling the switching variable uAB, which is expressed in

$$\int_{(n-1)T_s}^{nT_s} u_{AB}(t) i_l(t) dt = u_{ref} i_o(t) T_s + \int_{(n-1)T_s}^{nT_s} u_l(t) i_l(t) dt \qquad (n = 1,2 \ldots \ldots)$$

IMPLEMENTATION OF THE SCS

Calculation of the Control Reference Wout(n) + W(n)

As control reference, Wout(n) + W(n) should be calculated in the time instant of the beginning of the nth switching cycle and kept during the entire switching cycle. After measuring the variable io, Wout(n) is obtained by (13). And as we know, the energy is absorbed and released equally by the inductor in a switching cycle under the steady-state conditions. However, it is not equal under the dynamic state conditions, since the inductor current cannot change instantaneously. Therefore, to ensure the dynamic performances, W(n) should be considered and calculated as follows:

$$\Delta W_l(t) = \int_{(n-1)T_s}^{t} u_l(t) i_l(t) dt (t \in [(n-1)T_s, (n-1)T_s + T_s)])$$

where iis the measured variable, and uis obtained using

$$u_l(t) = L \frac{i_l(t+T_c) - i_l(t)}{T_c}$$

where Tc is the sampling cycle.

The state analysis shows that the inductor works during the entire switching cycle, which means the time t of (22) goes to the end of the nth switching cycle, therefore, W(n) is calculated by (14). Note here that the control reference is collected only in the time instant of the beginning of each switching cycle, therefore, W(n) used in the control reference of the nth switching cycle is actually W(n − 1) calculated in the (n − 1)th switching cycle, which means W(n) used in the SCS has a switching cycle lag.

Implementation Procedure of the SCS

After the computation of Wout(n) + W(n), the SCS can be implemented with simple logic functions (comparison and integration) as shown in Fig. 1. Here, the implementation for control of a CCM buck converter is described as follows: the integration process starts at the moment when S1 is turned ON by the fixed frequency clock pulse. At this moment, uAB(t) = uin(t) − usat. As time goes on, the integration value Wint(t) increases from its initial value shown in Fig. 2 as follows:

$$W_{int}(t) = \int_{(n-1)T_s}^{t} (u_{int}(t) - u_{sat}) i_l(t) dt + W_{initial}(n) \quad (t \in [(n-1)T_s, (n-1)T_s + T_s])$$

and Wint(t) compares with Wout(n)+ W(n) instantaneously. At the instance when Wint(t) reaches Wout(n) + W(n), the comparator generates a reset pulse to reset the RS flip-flop to be (Q = 0). Then switch S1 is changed from the ON-state to the OFF-state.

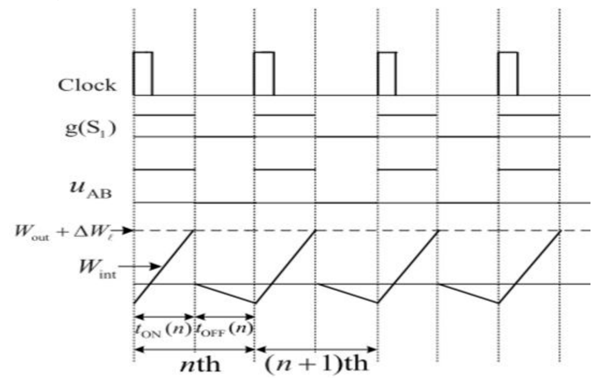

Fig :2 operation waveform of the SCS of the buck converter

where dSCS(n) is the duty ratio, which is tON(n)/ Ts, and Winitial(n) is the integration value during the OFF-state of S1, in this switching state, no energy is injected into the circuit, and uAB is equal to −ud. Then the integration restarts from zero with the value of −udi(t) after the reset, as shown in Fig. 2. The switch S1 is OFF until the arrival of the next clock pulse, which starts the (n + 1)th switching cycle. Thus

$$W_{initial}(n) = \int_{(n-1)T_s + d_{SCS}(n)T_s}^{nT_s} -u_d i_l(t) dt.$$

As the implementation for a DCM buck converter is similar to that of CCM, the details are not presented here

STEADY-S TATE ANALYSIS

Steady-State Operation

Analysis Under the steady-state conditions, the inductor absorbs and releases equal energy, which means W(t) = 0. Meanwhile, after reaching the steady state, i(t) is equal to io(t) by neglecting the current ripple. Thus, (21) becomes

$$\frac{1}{T_s}\int_{(n-1)T_s}^{(n-1)T_s+T_s} u_{AB}(t)dt = u_{ref}$$

from (21), it is observed that in each switching cycle, the average of the switching variable uAB(t) is exactly equal to the control reference uref, which ensures the tracking of the output voltage to uref in each switching cycle [8].

Stability Analysis

Under the steady state, neglecting W(t) since W(t) = 0 and the conduction losses of S1 and D1, (25) becomes

$$\frac{1}{T_s}\int_{(n-1)T_s}^{(n-1)T_s+d_{scs}(n)T_s} u_{in}(t)i_l(t)dt = u_{ref}i_o(t)$$

$$d_{scs}(n) = \frac{u_{ref}i_o(t)}{u_{in}(t)i_l(t)}$$

Then a buck converter with the SCS can be described by the following system of differential equations:

$$x(t) = Ax(t) + Bu_{in}(t)$$

$$d_{scs} = \frac{u_{ref}i_o(t)}{u_{in}(t)i_l(t)}$$

and R represents the parasitic resistance of the inductor (for simplicity, the parasitic resistance of C was neglected). A disturbance to the converter causes the changes uo(t) in the output voltage, i(t) in the inductor current, and d SCS in the duty ratio. System (29) can be rewritten in terms of disturbances

$$\widehat{x}(t) = A\hat{x}(t) + B_1 V_{in}$$

$$\widehat{d}_{scs} = \frac{V_{ref}}{RV_{in}I_l}\widehat{u}_0(t) - \frac{D}{I_l}\widehat{i}_l(t)$$

$$V = \frac{1}{2}L\widehat{i}_l^{2} + \frac{1}{2}C\widehat{u}_0^{2}$$

A Lyapunov function is defined as

$$\frac{dV}{dt} = L\widehat{i}_l\frac{d\widehat{i}_l}{dt} + C\widehat{u}_0\frac{d\widehat{u}_0}{dt}$$

It is obvious that ((Vref uo dSCS)/RD)<0, which satisfies the Lyapunov stability criterion [16], [17]. Hence, the SCS is stable.

ANALYSIS OF DYNAMIC RESPONSE

The capacitor voltage drop is reconsidered as uc(n) here for the analysis of the transient response. Since the dynamic performance under a load current change is arguably the most important issue in power converter design, the transient response to a positive load current change will be fully discussed. Referring to Fig. 3, immediately following the load current step change io1 → io2, the inductor current cannot

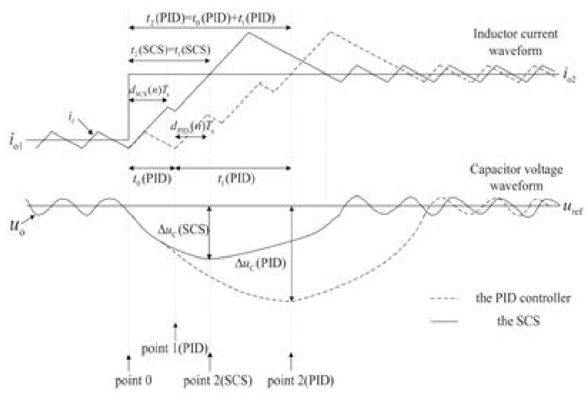

Fig :3 inductor current path of a buck converter under a positive load current step

change instantaneously to supply the step of the load current. Therefore, a portion of the load current must be supplied by the output capacitor. This, in turn, causes the output capacitor to lose charge and the output voltage to decrease. Before point 2, the inductor current is lower than the load current, the capacitor voltage continues to decrease. At point 2, the inductor current is equal to the load current, and then the capacitor stops discharging. At this point, the capacitor voltage drop is at its maximum, which is expressed in

$$C\frac{du_c(t)}{dt} = i_c(t) = i_l(t) - i_0(t)$$

$$\Delta u_c(n) = \frac{1}{c}\int_{point0}^{point2}\big(i_l(t) - i_0(t)\big)$$

Assuming the positive and negative inductor slews are invariable, in order to minimize uc(n), the duration t2, which represents the integral period (point 0–point 2), must be minimized. It means the inductor current ishould achieve the new load current as soon as possible. Here, three factors influence the inductor current to change:

1) the parameters of the circuits;
2) the delay time for responding to the disturbances;
3) the duty ratio during the increase of ifrom io1 to io2.

Under certain circuit parameters, the change of i is determined by the other two factors. First, when io steps from io1 to io2, the tON(n) and tOFF(n) of the SCS will be immediately allocated again according to (21); at the same time, the SCS makes the corresponding adjustments immediately to the switching pulses. However, using the current-mode PID controller, the load changes are firstly responded in the inductor current. Then the switching pulse is adjusted after the changes of the inductor current get to the comparator through the compensation block. This will bring an unpredictable latency t0, as shown in Fig. 3. Then, during the increase of i based on the given io, the bigger the duty ratio is, the more quickly igets to io2. The following is the calculations and comparison of the duty ratios.

The designing principle of the current-mode controller is that the inner current controller is designed by ignoring the influence of the output voltage and the outer voltage controller is designed under the assumption that the actual current completely tracks the reference current. This shows that, during t1 , the purpose that the inner and outer loops adjust the duty ratio is to offset the inductor voltage changes u(n), although the outer voltage loop implements this purpose by adjusting the uo. Thus, according to (37), the duty ratio dPID(n) is obtained as follows:

$$d_{PID}(n) = \frac{u_{ref}+\Delta u_l(n)}{u_{in}(t)} = \frac{u_{ref}}{u_{in}(t)} + \frac{\Delta u_l(n)}{u_{in}(t)}$$

because i(t) < io2(t) during t1 , the comparison between (36) and (38) shows that dSCS(n) is always greater than dPID(n) until i reaches io2. Therefore, uc(SCS) is smaller than uc(PID), as shown in Fig. 3. Since i using the SCS can approach the new output current io2 more quickly, the recovery time can be reduced in such a situation, as shown in Fig. 3. This is demonstrated in Fig. 4, which shows the simulation comparison results of the inductor current responses using the SCS and the PID controller to the load current step by changing the load from 8 to 4. The simulation results show that the inductor current using the SCS increases to the new steady-state output current very quickly. However, with the PID controller, the inductor current takes more than 16 ms to get to the new steady state. Under other transient conditions, the analysis is virtually similar to those detailed above.

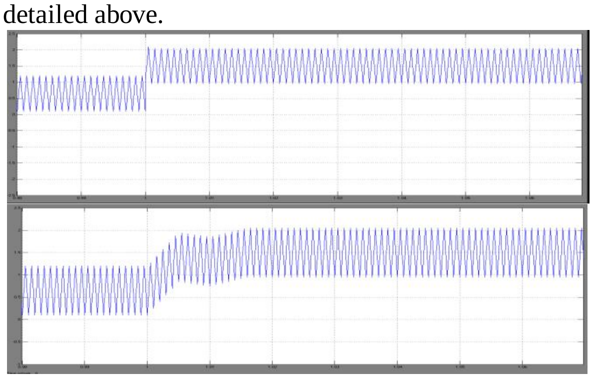

Fig :4 responses of the inductor current to a positive load current step

SIMULATION RESULTS

Simulation and experimental results are used to demonstrate the superior performances of the SCS. For simulation studies, buck converter A with the low switching frequency fs = 1 kHz and buck converter B with the high switching frequency fs = 40 kHz are configured. To evaluate the performances of the SCS, the following section presents a comparative study with a current-mode PID controller. A comparison is made with a current-mode controller because it is most frequently used in voltage regulator module (VRM) applications.

According to the circuit shown in Fig. 1, buck converter A has the parameters: uin = 15 V, uref = 6 V, u pp = 0.08 V, R = 8, L = 2500 μH (CCM)/ 800 μH (DCM), C = 1200 μF (CCM)/2200 μF (DCM). The inductances and capacitances are determined by the following equations:

$$L_{(critical)} = \frac{u_{ref}(1-d)}{2i_{o(min)}f_s}$$

$$C = \frac{u_{ref}(1-d)}{8\Delta u_{pp}Lf^2{}_s}$$

where L (critical) represents the critical inductance between CCM and DCM; L represents the inductance determined according L(critical). The PID controllers are designed by the SISO tool of MATLAB with the crossing frequency of 192 Hz and the phase margin of 50.3°.

Figs. 5–8 show the responses of buck converter A working in CCM and DCM undergoing step changes of the load current and input voltage. In Fig. 5, the responses to the load current steps of CCM buck converter A are compared with that of the PID controller. The results show that under the positive

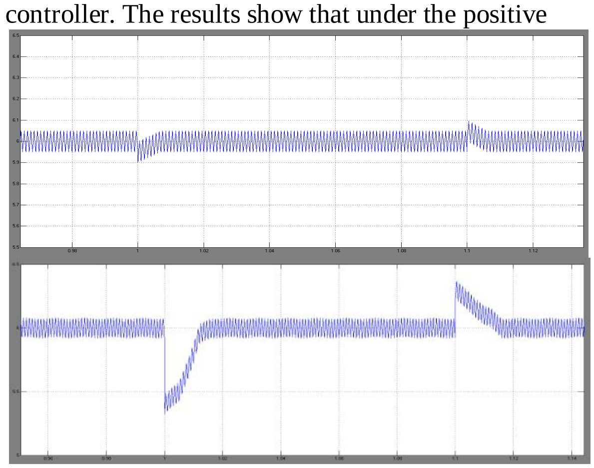

Fig :5 simulation result of a output voltage respone to the load current change for the buck converter a working in CCM

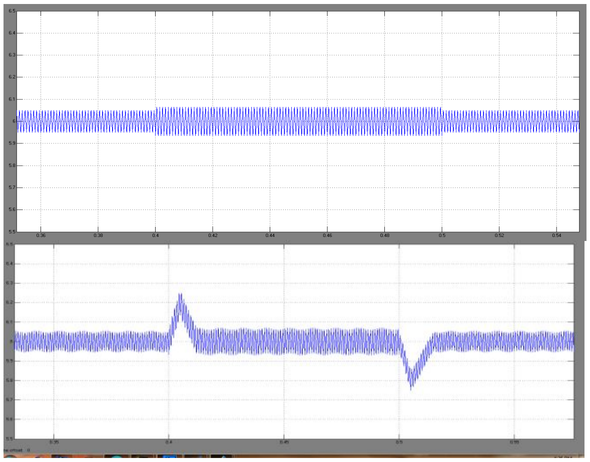

Fig :6 simulation result of output voltage response to the input voltage change (15 V→18V→12V) for buck converter a working in CCM

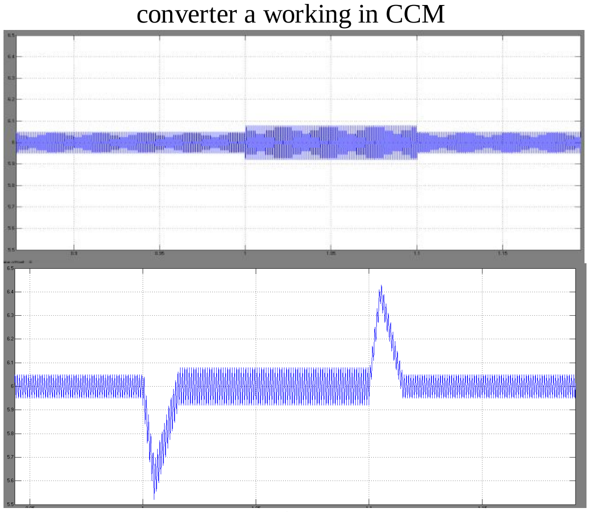

Fig :7 simulation result of output voltage response to the load current change for buck converter a working in DCM

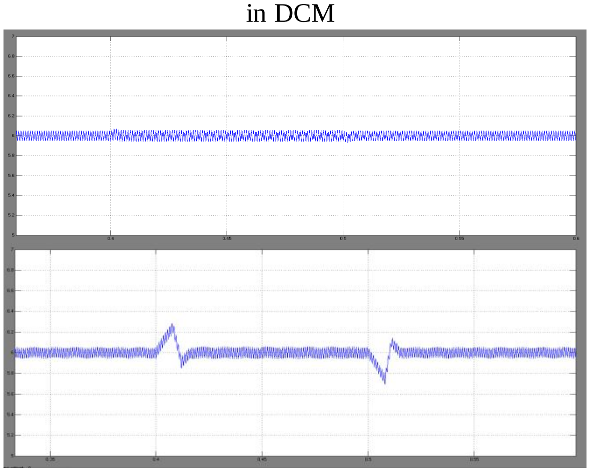

Fig :8 simulation result of output voltage response to the input voltage change (15 V→18V→12V) for buck converter a working in DCM

current step change by changing the load from 8 to 4, the voltage peak undershoot uo is reduced from −0.35 (with the PID controller) to −0.1 V (with the SCS) and the settling time t settling is reduced from 16 ms to 7 ms.

Table :1
Simulationresults Ofbuckconverterainall Thedynamiccase

disturbance (R or u_{in})	SCS		PID	
	Δu_o	$t_{settling}$	Δu_o	$t_{settling}$
8 Ω → 4 Ω → 8 Ω (CCM)	-0.1 V / 0.05 V	7 ms / 6 ms	-0.35 V / 0.4 V	16 ms / 15 ms
15 V→ 18 V → 12 V (CCM)	0.02 V / -0.03 V	2 ms / 3 ms	0.2 V / -0.2 V	12 ms / 15 ms
8 Ω → 4 Ω → 8 Ω (DCM)	0 V / 0 V	0 ms / 0 ms	-0.4 V / 0.38 V	16 ms / 15 ms
15V→ 18V → 12V (DCM)	0.05 V / -0.03 V	3 ms / 2 ms	0.25 V / -0.15 V	16 ms / 15 ms

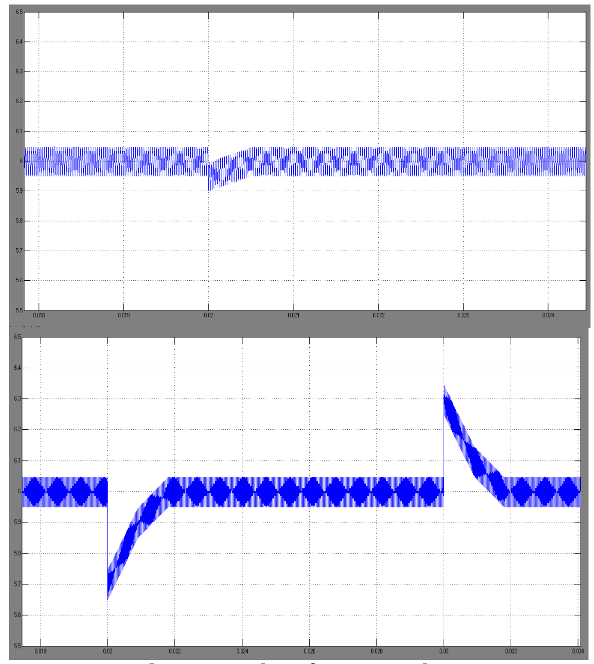

Fig. 9. Simulation results of output voltage response to the load current changes for the buck converter B working in CCM

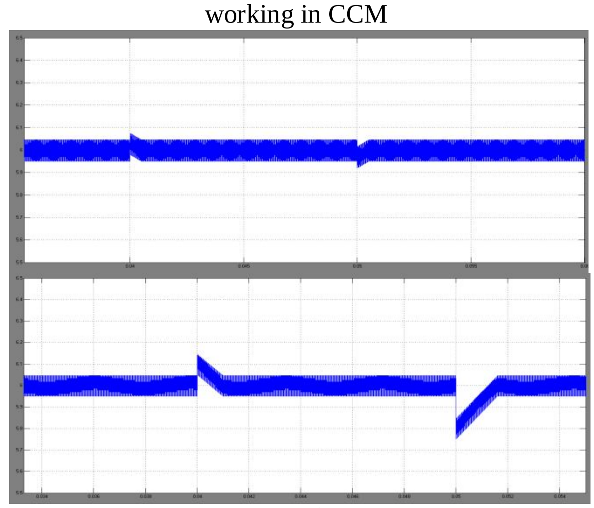

Fig. 10. Simulation results of output voltage response to the input voltage changes (15 V→18 V→12 V) for buck converter B working in CCM.

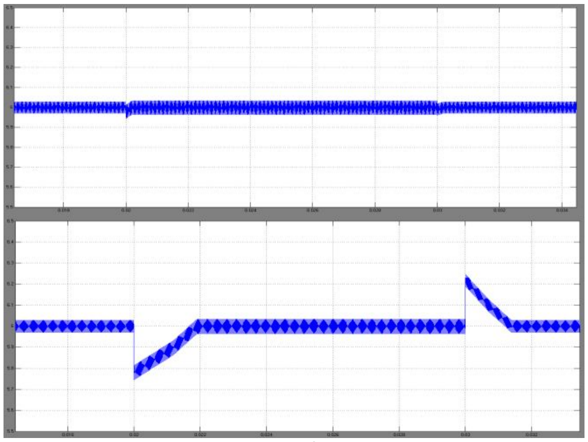

Fig. 11. Simulation results of output voltage response to the load current changes for buck converter B working in DCM.

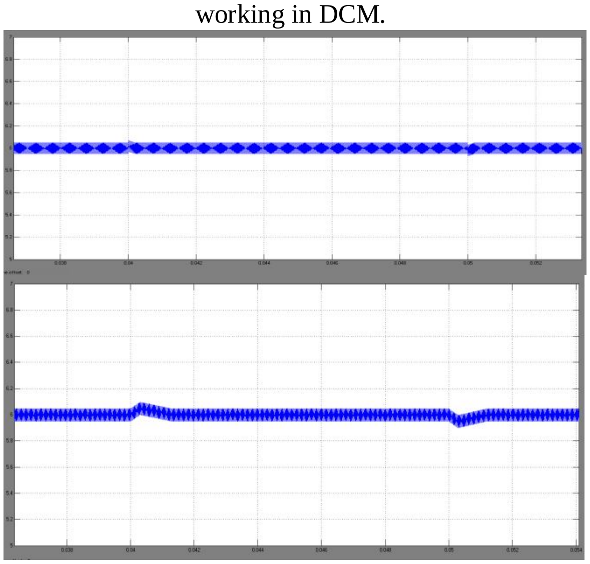

Fig. 12. Simulation results of output voltage response to the input voltage changes (15 V→18 V→12 V) for buck converter B working in DCM

Table I summarizes the simulation comparison results of the responses of the SCS and the PID controller to all the dynamic cases. It is observed from Table I that, compared with the PID controller, the voltage peak shoot uo and the settling time t settling with the SCS are significantly reduced in all cases.

In order to further verify the functionality of the SCS, a buck converter B is configured with the parameters: uin = 15 V, uref = 6 V, upp = 0.08 V, R = 8, L = 40 μH (CCM)/20 μH (DCM), C = 100 μF (CCM)/ 150 μF (DCM). The PID controllers are designed by the SISO Tool of MATLAB with the crossing frequency of 6 kHz and the phase margin of 62°. Figs. 9–12 show the simulation waveforms of the buck converter B under CCM operation and DCM operation, respectively. And the comparison results of the voltage shoot and settling time are summarized in Table II. The simulation results demonstrate that the SCS still has improved dynamic performances when the switching frequency increased to 40 kHz.

Table 2

Simulation results of buck converter B in all the dynamic cases

disturbance (R or u_{in})	SCS		PID	
	Δu_o	$t_{settling}$	Δu_o	$t_{settling}$
8 Ω → 4 Ω → 8 Ω (CCM)	-0.05 V / 0.1 V	0.5 ms /0.3 ms	-0.3 V /0.2 V	1.8 ms /1.8 ms
15 V→ 18 V → 12 V (CCM)	0.01 V / -0.03 V	0.1 ms / 0.4 ms	0.08 V / -0.2 V	0.8 ms / 1.6 ms
8 Ω → 4 Ω → 8 Ω (DCM)	-0.05 V / 0 V	0.2 ms / 0.5 ms	-0.22 V / 0.21 V	1.9 ms / 1.4 ms
15 V→ 18 V → 12 V (DCM)	0.03 V / -0.01 V	0.3 ms / 0.2 ms	0.08 V / -0.08 V	1.3 ms / 1.2 ms

CONCLUSION

The SCS is based on the energy conservation principle in circuit and it has been designed and implemented to control buck converters. The SCS is capable of operating in both CCM and DCM. And it has a simple structure, which can be easily implemented. Furthermore, the stability of the converter controlled by the SCS has been proved using Lyapunov stability criterion. The dynamic response to a positive load current step change demonstrates the SCS has superior dynamic performances. Simulation and experimental results show that compared with the PID controller, the SCS produces superior dynamic performance, in terms of smaller voltage shoots and shorter settling times under the step changes of input voltage and load current. These results demonstrate that the SCS can be a substitute for classic controllers in power converter applications where a quick dynamic response is required. In addition, the SCS is here discussed for the buck converters and it can be easily extended to other converter topologies, such as boost converters, buck-boost converters and even inverters, which will be reported in the future.

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