

A New VLSI Architecture of Power Efficient Nonvolatile Lookup Table Design Based on RRAM

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Abstract: Emerging non-volatile memories (NVMs), such as MRAM, PRAM, and RRAM have been widely investigated to replace SRAM and the configuration bits in field-programmable gate arrays (FPGAs) for high security and instant power ON. However, the variations inherent in NVMs and advanced logic process bring reliability issue to FPGAs. A single-stage sense amplifier with voltage clamp is employed to reduce the power and area without impairing the reliability. Matched reference path is proposed to reduce the parasitic RC mismatch for reliable sensing. RRAM is adopted as the configuration bit and the reference resistor to provide large sense margin, thus all aviating the effects of memory and logic process variations. By evaluation, remarkable improvements in power, delay, area, and reliability can be obtained. The extension for the project is quaternary look up table.

Keywords: low power, high speed, RRAM, FPGA- (Field Programmable Gate Array), non-volatile SRAM (nvSRAM).

I. INTRODUCTION

Basic NVMs, such as MRAM, PRAM, and RRAM, have been verified with better scalability and logic compatibility. Based on the logic-in-memory concept, lookup table, which is the core building block in FPGAs, has been introduced with non-volatility. First, various nonvolatile SRAM (nvSRAM) structures with MRAM and RRAM were proposed to directly replace SRAM in the traditional lookup table to acquire non-volatility. However, the size of nvSRAM cell is remarkably larger than that of SRAM, and the write disturbance is also difficult to avoid for half-select RRAM cells. Look up Table combined with NVM method has been proposed. Various NVSRAM with MRAM and RRAM replaces SRAM. But the drawback

is that the area requirement is more in the approach. It has been proposed that a 2 input Nonvolatile memory Look Up Table for run-time reconfiguration. Third type is a hybrid-LUT for MRAM. Drawback -Roff/Ron for MRAM which results in less sense margin and larger area. It has larger Roff/Ron ratio 1T1RAM cell has been used as the configuration bit and a reference resistor has been used to provide sufficient sense margin. Single-stage amplifier with voltage clamp is employed to reduce power and area. MRP has been devised to reduce parasitic RC mismatch between selected path in MUX and reference path for reliable sensing against logic variation, lowpower, high area efficiency, and low leakage at the same time.

Resistive Random Access Memory (RRAM)

This prototype consists of a traditional island-style FPGA (Field Programmable Gate Array)-fabricated in 90nm CMOS technology, on top of which the programmable resistors are integrated. Apart from the configuration memory, all other parts are constructed purely with CMOS transistors. The memory array is interleaved with the CMOS logic throughout the tile. Write drivers, row and columns decoders and sense amplifiers are shared by the FPGA tiles. Memory cells are constructed using a 1T2R topology, in which two programmable resistances (or PRs) behave as a voltage divider, pulling the bit line – connected to the cell through the access transistor – up or down. RRAM PRs are small when compared to the CMOS feature size, allowing for an optimized cell surface of only 24 F².

FPGAs

An FPGA (Field Programmable Gate Array)

is a reprogrammable chip which contains hundreds of thousands of logic gates that internally connects together to build complex digital circuitry. There are few steps given below. It is primarily a semiconductor device that can be configured by the user (customer or designer) after the manufacturing process has been completed. The term “field-programmable” means the device is programmed by the customer, not the manufacturer. It offers partial re-configuration of a portion of design.

SINGLE STAGE SENSE VOLTAGE AMPLIFIER:

It has low power dissipation and a sense of basic differential amplifier in comparison to the offset voltage. The differential voltage sensing operation, providing fast loading equipment for simultaneous exchange of meaning is the primary purpose of the amplifier. SSAVC rail-to-rail voltage logic state changes the resistance of the RRAM. Outb the low end and the output clock is the clock even more sense when the pre-charge to VDD. CLK charges a capacitor or a waste of considerable power, as a result, when discharged to the ground. The sense amplifier may suffer reduced clamp voltage currents, large ROFF / RRAM Ron still without impairing the validity of the concept helps to preserve the margin. Compared with the previous two-stage sense amplifier, a single-stage realization of an area of the lower die. M7 and M8 on the gates of the clamp voltage Vbias, VDD is less than that applied to the inside of the selected nodes in the TMUX and MRP only ($V_{bias} > V_{th}$) to be pre-charged.

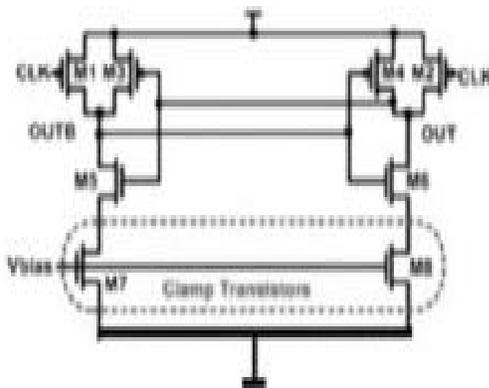


Figure 1: Single-Stage Sense Amplifier with Voltage Clamp.

DESIGN OF SINGLE STAGE SENSE AMPLIFIER WITH VOLTAGE CLAMP.

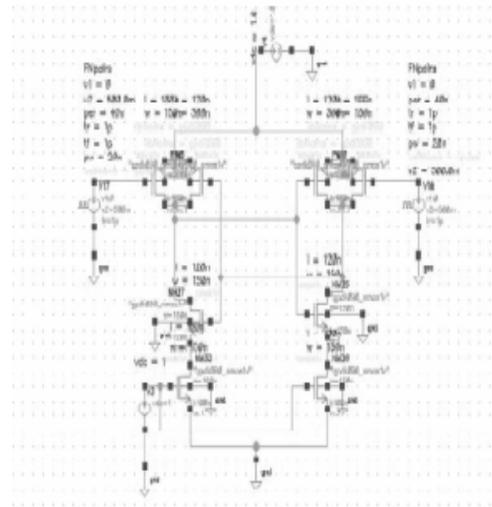


Figure 2: Schematic of single-stage sense amplifier with voltage clamp

II.Literature Survey

Such MRAM, PROM, and RRAM emerging NVMs, good quality and logic compatibility has been confirmed. FPGAs in the core building block of logic-in-memory concept, but inconsistency has been proposed based on the lookup table. First, MRAM and RRAM various nonvolatile SRAM (nvSRAM) structures have been proposed to replace the nonvolatile SRAM to achieve the classic look of the table. However, nvSRAM substantially larger than the cell size of the SRAM, and the writing half of the selected disturbance RRAM cells is also difficult to avoid. For MRAM, Suzuki et al. Nonvolatile two-input lookup table (nvLUT) low-power current-mode logic is based on the proposed MRAM. Suzuki et al. Also acquire sufficient sensing margin of serial / parallel magnetic junctions nvLUT proposed a six input. Zhao et al. NvLUT proposed another MRAM-based run-time reconfiguration. LUT2 hybrid Wren proposed a third type of MRAM-based nvLUT. However, MRAM's ROFF / RON small PRAM or RRAM, the serial / parallel magnetic junctions, seems low compared to the margin, or as a result of a large area.

III. Proposed System

To illustrate the proposed design, the input nvLUT presented as shown in Fig. 1. The input is all too easily be extended to six in the current mainstream

FPGA products. the format of nvLUT SSAVC, a tree Multiplexer (TMUX), a MRP, a RRAM piece, and will have an footer transistor. RRAM as a reference resistor blanks at the right-most slice of the RRAM cell configuration forms for the left and four 1T1R RRAM cells.

LOW POWER VARIATION TOLERANT NVLUT

To illustrate the design, the input nvLUT presented as shown in Fig. 3, the input count is even easier FPGA products in the main stream of the six, expanded. Of the total construction nvLUT a SSAVC, a tree Multiplexer (TMUX), a MRP, a RRAM piece, and will have an footer transistor. RRAM as a reference resistor blanks at the right-most slice of the RRAM cell configuration forms for the left and four 1T1R RRAM cells. The truth table logic voltage SRAM is different from the resistance of the state, ROFF or RON, will be stored in the form of a piece of RRAM. For example, a NOR gate, in order to nvLUT program, R0 RON 1, as indicated, R1, R2, and R3 ROFF represents 0. The inputs IN0 and IN1 TMUX of the RRAM cell to select the program to the program. RRT in the sense amplifier to the output 1 to be exposed to high parasitic RC bit and reference resistor, making the configuration of the memory margin between the resistance variation is subtle, reference may be slow discharge path.

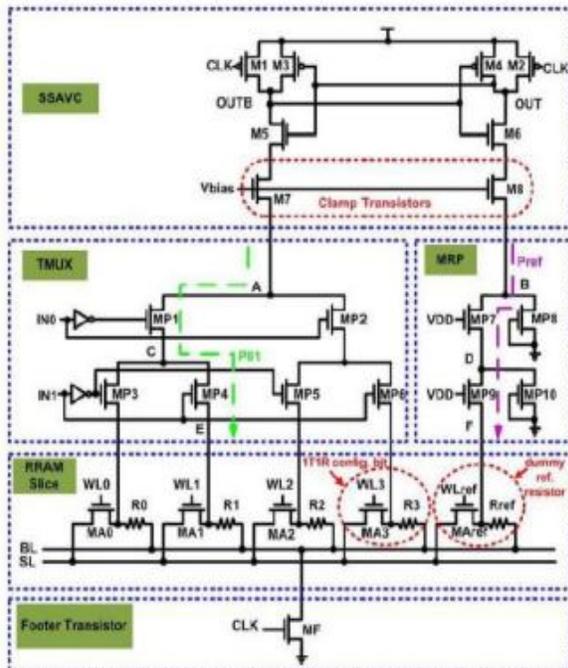


Fig 3: Overall architecture of the proposed low-power variation nvLUT based on RRAM

RRAM as a Configuration Bit and a Reference Resistor

The 1T1R RRAM cell is employed as a configuration bit and a reference resistor to provide sufficient sense margin, as shown in Fig 3. Different from crossbar array, a 1T1R RRAM cell can eliminate the sneaking current and the disturbances during write and read, thus saving power and acquiring high yield. The typical RON and ROFF of RRAM are of kilo-ohms and mega ohms, respectively, and ROFF/RON is over 100, which is at least 40× larger than that of MRAM. Therefore, sufficient sense margin is guaranteed and the configuration resources are also saved by half compared with the parallel or serial combination scheme. Moreover, the RRAM storage layer, i.e., R0-3 and R ref, is stacked in the back-end of line without occupying an additional area, as shown fig 4

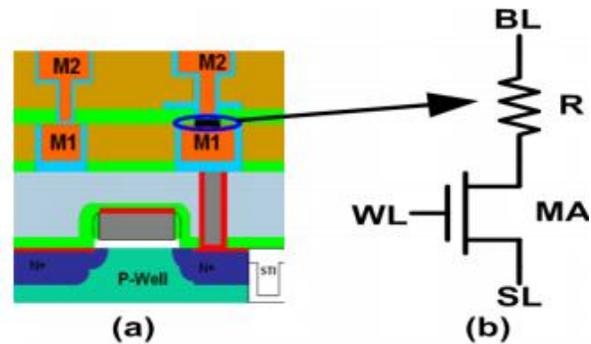


Fig 4: 1T1R RRAM cell integration process and structure. (a) Cross-sectional view. (b) Schematic.

Because the characteristics of RRAM are different from conventional resistor, the sense margins of RON and ROFF compared with a conventional reference resistor may suffer asymmetric changes under memory and logic process variation, which may result in read failure. To resolve this issue, dummy RRAM cell, which is programmed to a mid state resistance, is adopted as the reference resistor. Thus, the configuration bits and reference resistor vary in the same way across different temperatures and process conditions, preserving the sense margins for both RON and ROFF. Moreover, the dummy cell occupies less area than conventional resistors. The peripheral decoding and writing circuits for dummy cell can also be shared with configuration bits, bringing less area overhead.

Single Stage Sense Voltage Amplifier

It has low power dissipation and a sense of basic

differential amplifier in comparison to the offset voltage. The simultaneous exchange of equipment, providing fast load-sensing operation, the sense voltage Differential is the primary purpose of the amplifier. SSAVC rail-to-rail voltage logic state changes the resistance of the RRAM. Out the low end and the output clock is the clock even more sense when the pre charge to VDD. CLK considerable power to the ground with a capacitor or waste, as a result, when the discharge level. The sense amplifier may suffer reduced clamp voltage currents, large ROFF / RRAM Ron still without impairing the validity of the concept helps to preserve the margin. Compared with the previous two-stage sense amplifier, a single-stage realization of an area of the lower die. The clamp voltage Bias, to be implemented M7 and M8 on the gates, TMUX, MRP the selected path and the inner nodes (V bias, Vth) can only pre charged to, VDD is less than.

RRAM Slice:

It constitutes of four ITIR RRAM cells at the left for configuration and a dummy RRAM cell at the right most as a reference resistor. The truth table is stored in the RRAM slice in the form of resistance state, ROFF or RON, which is different from the logic voltage in SRAM.

Footer Transistor.

The function of footer transistor mf is to allow current to flow during sensing and it is closed during pre charge to restrain leakage.

MRP (Matched Referenced Path):

Although trimming Rref by SAWM can help to disabuse the parasitic resistance mismatch between the selected path in TMUX and reference path, their parasitic capacitance mismatch cannot be easily estimated and compensated. The MRP is devised to minimize the parasitic RC mismatch between the above-mentioned two paths. To illustrate this point, IN0 and IN1 are assumed to take the logic values of 0 and 1, respectively. The path marked by the green dash line in TMUX, P01, is selected to be compared with the reference path, Pref, For reliable sensing, the parasitic RCs of P01 and Pref should be equivalent. Therefore, the transistors MP8 and MP10 with their gate grounded are, respectively, added at the nodes B and D in MRP to imitate the parasitic effects of OFF-state transistors MP2 and MP3 at the nodes A and C in TMUX. Moreover, the transistors in MRP take the

same size with the pass transistors in TMUX. The proposed MRP has the same parasitic RC with the selected path in TMUX, while RRT has more parasitic RC. The excessive parasitic RC in RRT may slow down the discharging of the reference path, making th3 sense amplifier prone to output 1 when the resistance margin between the configuration bit and the reference resistor is subtle due to memory variation.

TMUX (Terminal Multiplexer):

TMUX is a multiplexer with select line in0 and in1 which are used to select the corresponding RRAM. Its working principle is similar to NOR operation.

IV. Extension

A quaternary variable can assume four different logic levels. Assuming a rail-to-rail voltage range and equal noise margins for the four logic levels, three different reference voltage values are required, 1/6VDD, 3/6VDD, and 5/6VDD, to determine a quaternary value. This is shown in Fig. 1. Since a quaternary variable (Q) is able to carry twice as much information as a binary variable (B), we have the following relation:

$$|Q| = 2 \times |B|.$$

Therefore, two binary variables may be grouped into one quaternary variable without information loss, merging two nodes into one. It should be noted that there is no direct conversion of binary to quaternary logic gates in conventional CMOS, since the binary circuits use the available power rails to represent the binary symbols. For quaternary logic there are two more intermediate levels, which cannot be obtained directly using the same techniques. On the other hand, viable implementations of quaternary circuits have already been achieved for LUTs, as demonstrated in [9]. A LUT is an array indexing operator, where the output is mapped by the input, based on the configuration memory. The configuration values are initially stored in the LUT configuration memory, and according to the input, the logic value in the addressed position is assigned to the output. By properly programming the LUT configuration memory, the LUT can implement any logic function with the given number of inputs and outputs, making it very practical to implement reconfigurable hardware, such as FPGAs.

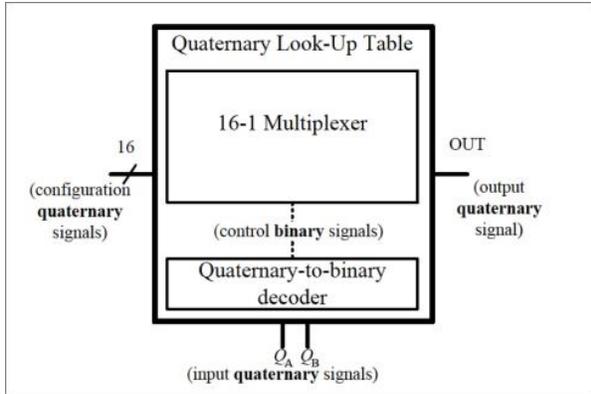


Fig.5. quaternary LUT.

V. Simulation Results

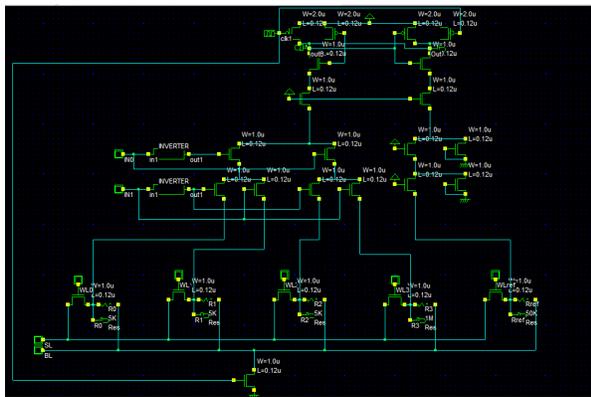


Fig 6: RRAM based two -input nvLUT

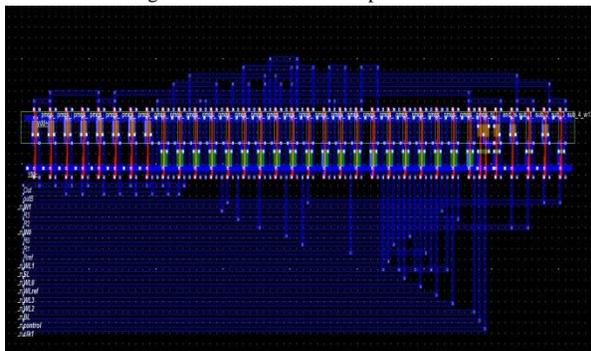
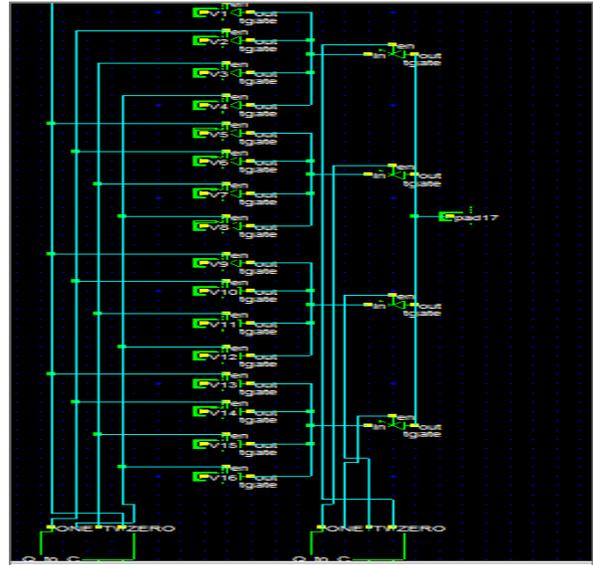


Fig7. Layout diagram for RRAM based two -input nvLUT.

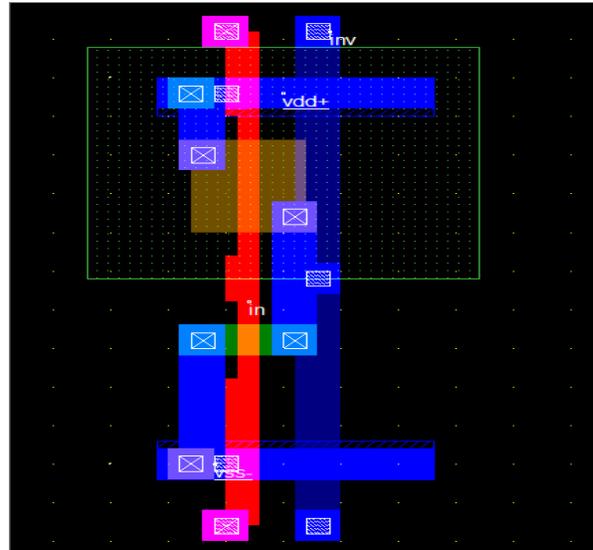


Fig 8. Voltage VS Time diagram for RRAM based two -input nvLUT.

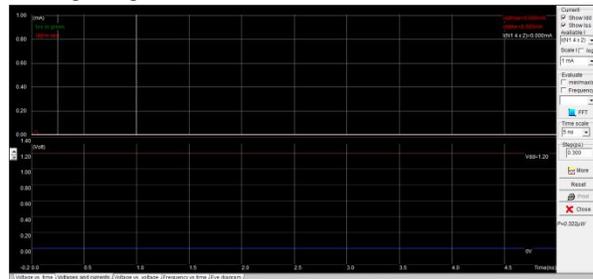
Extension.
Schematic.



Layout Design.



Timing Diagram.



V. Conclusion

The design techniques of high density asynchronous look up table based on RRAM is described. RRAM is adopted as the configuration bit

and the reference resistor to provide large sense margin, thus alleviating the effects of memory and logic process variations. Because of the high ROFF/RON of RRAM, SSAVC helps to reduce the power and area without impairing the reliability. The MRP is also devised to reduce the parasitic RC mismatch between the selected path in the multiplexer and the reference path for reliable operation.

REFERENCES

- [1] S.D.Brown, R.J.Francis, J.Rose, and Z.G.Vranesic, *Field Programmable Gate Arrays*. Boston, MA, USA: Kluwer, 1992.
- [2] S. Seo et al., "Reproducible resistance switching in polycrystalline NiO films," *Appl. Phys. Lett.*, vol. 85, no. 23, pp. 5655–5657, 2004.
- [3] L. Torres, R. M. Brum, L. V. Cargnini, and G. Sassatelli, "Trends on the application of emerging nonvolatile memory to processors and programmable devices," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2013, pp. 101–104.
- [4] M. Wanget al., "A novel CuxSiyO resistive memory in logic technology with excellent data retention and resistance distribution for embedded applications," in *Proc. Symp. VLSI Technol. (VLSIT)*, Jun. 2010, pp. 89–90.
- [5] X. Xue et al., "Nonvolatile SRAM cell based on CuxO," in *Proc. 9th Int. Conf. Solid-State Integr.-Circuit Technol. (ICSICT)*, Oct. 2008, pp. 869–871.
- [6] N. Bruchon, L. Torres, G. Sassatelli, and G. Cambon, "Technological hybridization for efficient runtime reconfigurable FPGAs," in *Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI)*, Mar. 2007, pp. 29–34.
- [7] W. Zhao, E. Belhaire, B. Dieny, G. Prenat, and C. Chappert, "TAS-MRAM based non-volatile FPGA logic circuit," in *Proc. Int. Conf. Field-Program. Technol. (ICFPT)*, Dec. 2007, pp. 153–160.
- [8] D. Suzuki et al., "Fabrication of a nonvolatile lookup-table circuit chip using magneto/semiconductor-hybrid structure for an immediate power-up field programmable gate array," in *Proc. Symp. VLSI Circuits (VLSIC)*, Jun. 2009, pp. 80–81.
- [9] D. Suzuki, M. Natsui, T. Endoh, H. Ohno, and T. Hanyu, "Six-input lookup table circuit with 62% fewer transistors using nonvolatile logic-in-memory architecture with series/parallel-connected magnetic tunnel junctions," *J. Appl. Phys.*, vol. 111, no. 7, pp. 07E318-1–07E318-3, 2012.
- [10] W. Zhao, E. Belhaire, C. Chappert, and P. Mazoyer, "Power and area optimization for run-time reconfiguration system on programmable chip based on magnetic random access memory," *IEEE Trans. Magn.*, vol. 45, no. 2, pp. 776–780, Feb. 2009.
- [11] F. Ren, "Energy-performance characterization of CMOS/magnetic tunnel junction (MTJ) hybrid logic circuits," M.S.

thesis, Dept. Elect. Eng., Univ. California, Los Angeles, CA, USA, 2011.

- [12] T. Sakamoto et al., "A nonvolatile programmable solid electrolyte nanometer switch," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2004, pp. 290–529