A Novel Design of High-Speed Carry Skip Adder Operating Under a Wide Range of Supply Voltages

Jalluri Srinivisu, (M.Tech), Email Id: jsvasu494@gmail.com
Ch. Prabhakar, M.tech, Assoc. Prof, Email Id: skytechsolutions2015@gmail.com

Bhimavaram Institute of Engineering & Technology, Pennad(V), Palakoderu(M), West Godavari (D), Andhra Pradesh, Pin code: 534243.

Abstract: In this paper, we implemented a carry skip adder (CSKA) structure that has a higher speed and lower energy consumption compared with the conventional one. The speed enhancement is achieved by applying concatenation and instrumentation schemes to improve the efficiency of the conventional CSKA (Conv CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles. Finally, a hybrid variable latency extension of the proposed structure, which lowers the power consumption without considerably impacting the speed, is presented.

Keywords: CSKA, hybrid structure, AOI, OAI.

I. Introduction

Adders are a key building block in arithmetic and logic units (ALUs) and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units, which have been reported. Obviously, it is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage. Moreover, the sub threshold current, which is the main leakage component in OFF devices, has an exponential dependence on the supply voltage level through the drain-induced barrier lowering effect. Depending on the amount of the supply voltage reduction, the operation of ON devices may reside in the super threshold, near-threshold, or sub threshold regions. Working in the super threshold region provides us with lower delay and higher switching and leakage powers compared with the near/sub threshold regions. In the sub threshold region, the logic gate delay and leakage power exhibit exponential dependences on the supply and threshold voltages. Moreover, these voltages are (potentially) subject to process and environmental variations in the Nano scale technologies. The variations increase uncertainties in the aforesaid performance parameters. In addition, the small sub threshold current causes a large delay for the circuits operating in the sub threshold region. Recently, the near-threshold region has been considered as a region that provides a more desirable tradeoff point between delay and power dissipation compared with that of the sub threshold one, because it results in lower delay compared with the sub threshold region and significantly lowers switching and leakage powers compared with the
super threshold region. In addition, near-threshold operation, which uses supply voltage levels near the threshold voltage of transistors, suffers considerably less from the process and environmental variations compared with the sub threshold region. The dependence of the power (and performance) on the supply voltage has been the motivation for design of circuits with the feature of dynamic voltage and frequency scaling. In these circuits, to reduce the energy consumption, the system may change the voltage (and frequency) of the circuit based on the workload requirement. For these systems, the circuit should be able to operate under a wide range of supply voltage levels. Of course, achieving higher speeds at lower supply voltages for the computational blocks, with the adder as one the main components, could be crucial in the design of high-speed, yet energy efficient, processors. In addition to the knob of the supply voltage, one may choose between different adder structures/families for optimizing power and speed. There are many adder families with different delays, power consumptions, and area usages. Examples include ripple carry adder (RCA), carry increment adder (CIA), carry skip adder (CSKA), carry select adder (CSLA), and parallel prefix adders (PPAs). The descriptions of each of these adder architectures along with their characteristics may be found. The RCA has the simplest structure with the smallest area and power consumption but with the worst critical path delay. In the CSLA, the speed, power consumption, and area usages are considerably larger than those of the RCA. The PPAs, which are also called carry look-ahead adders, exploit direct parallel prefix structures to generate the carry as fast as possible. There are different types of the parallel prefix algorithms that lead to different PPA structures with different performances. As an example, the Kogge–Stone adder (KSA) is one of the fastest structures but results in large power consumption and area usage. It should be noted that the structure complexities of PPAs are more than those of other adder schemes. The CSKA, which is an efficient adder in terms of power consumption and area usage, was introduced. The critical path delay of the CSKA is much smaller than the one in the RCA, whereas its area and power consumption are similar to those of the RCA. In addition, the power-delay product (PDP) of the CSKA is smaller than those of the CSLA and PPA structures. In addition, due to the small number of transistors, the CSKA benefits from relatively short wiring lengths as well as a regular and simple layout. The comparatively lower speed of this adder structure, however, limits its use for high-speed applications.

II. Literature Review

Existing design considered a design of efficient adder circuits based on a conservative reversible logic gate. Here, a 4-bit reversible carry skip adder is presented using gates. This design needs so many gates for the full circuit. As a result, this design is not optimized in terms of delay. The same design paradigm, while their circuit was designed using different types of gates. These designs require a huge number of gates and garbage outputs. Moreover, these designs didn’t show the quantum realization of the circuit. So, the delay of the quantum circuits and quantum gate calculation complexities were absent in these works.

This paper presents the design of a novel n-bit carry skip adder by its core components using quantum logic. The novelty of the proposed adder is that it considers a new design with optimal delay. Moreover, it is the first time in quantum circuit synthesis that the quantum realization of a carry skip adder is shown in terms of quantum gates, power and area, etc. Our proposed quantum multiplexer gate (QMG) and quantum comparison gate (QCG) perfectly operates as a 2-to-1 MUX and a comparison circuit, respectively. Using QMG and QCG as a unit element of construction, we optimize the
design of Carry Skip Adder. A generalized architecture of the proposed n-bit adder has also been presented. The comparative study shows that the proposed quantum carry skip adder performs better than the existing carry skip adders with the increasing number of bits; e.g., the proposed 128-bit carry skip adder improves 40.96% on number of quantum gates, 48.19% on delay, 22.22% on garbage outputs and 40.96% on area and power over the existing best one. In addition, we also simulate the proposed adder using Microwind and DSCH 3.5 software to show the correctness of the circuit.

A new modified Manchester carry chain (MCC) is presented. The objective is to reduce the carry propagation delay in the chain obtaining a layout-oriented architecture. The modification provides bypass (carry-skip) routes for the carry to propagate through quickly, avoiding long carry propagation paths that go through the entire carry chain. When realized using AMS 0.35mm2-poly 3-metal 3.3V CMOS technology (CSD), a 32-bit adder designed as described here shows a computational delay of about 2.2 ns and an energy dissipation of only 27 pJ. This represents a significant improvement in terms of energy–delay product with respect to both conventional MCC adders and newer adder structures.

In this paper, the impact of different dynamic logic design styles is evaluated considering as benchmark a fast carry skip adder. Four different adder designs were implemented in standard domino, footless domino, data driven dynamic, and dynamic hybrid (standard domino + data driven dynamic) logic design styles, by exploiting the STMicroelectronics 45nm 1V CMOS technology. When applied to a 32-bit carry-skip adder, the data driven dynamic approach assures an energy-delay product 29%, 33% and 39% lower than the standard domino, footless domino, and dynamic hybrid implementations, respectively.

III. Existing system

The conventional structure of the CSKA consists of stages containing chain of full adders (FAs) (RCA block) and 2:1 multiplexer (carry skip logic). The RCA blocks are connected to each other through 2:1 multiplexers, which can be placed into one or more level structures. The CSKA configuration (i.e., the number of the FAs per stage) has a great impact on the speed of this type of adder. Many methods have been suggested for finding the optimum number of the FAs. The techniques presented use of VSSs to minimize the delay of adders based on single level carry skip logic. In some methods to increase the speed of the multilevel CSKAs are proposed. The techniques, however, cause area and power increase considerably and less regular layout. The design of a static CMOS CSKA where the stages of the CSKA have a variable sizes was suggested.

In addition, to lower the propagation delay of the adder, in each stage, the carry look-ahead logics were utilized. Again, it had a complex layout as well as large power consumption and area usage. In addition, the design approach, which was presented only for the 32-bit adder, was not general to be applied for structures with different bits lengths. Alioto and Palumbo propose a simple strategy for the design of a single-level CSKA. The method is based on the VSS technique where the near-optimal numbers of the FAs are determined based on the skip time (delay of the multiplexer), and the ripple time (the time required by a carry to ripple through a FA).

The goal of this method is to decrease the critical path delay by considering a non integer ratio of the skip time to the ripple time on contrary to most of the previous works, which considered an integer ratio. In all of the works reviewed so far, the focus was on the speed, while the power consumption and area usage of the CSKAs were not considered. Even for the speed, the delay of skip logics, which are based on multiplexers and
form a large part of the adder critical path delay, has not been reduced.

![Fig 1: Conventional Structure of the CSKA.](image)

**Improving Efficiency of Adders at Low Supply Voltages:**

To improve the performance of the adder structures at low supply voltage levels, some methods have been proposed an adaptive clock stretching operation has been suggested. The method is based on the observation that the critical paths in adder units are rarely activated. Therefore, the slack time between the critical paths and the off-critical paths may be used to reduce the supply voltage. Notice that the voltage reduction must not increase the delays of the noncritical timing paths to become larger than the period of the clock allowing us to keep the original clock frequency at a reduced supply voltage level. When the critical timing paths in the adder are activated, the structure uses two clock cycles to complete the operation. This way the power consumption reduces considerably at the cost of rather small throughput degradation. The efficiency of this method for reducing the power consumption of the RCA structure has been demonstrated.

The CSLA structure was enhanced to use adaptive clock stretching operation where the enhanced structure was called cascade CSLA (C<sup>2</sup>SLA). Compared with the common CSLA structure, C<sup>2</sup>SLA uses more and different sizes of RCA blocks. Since the slack time between the critical timing paths and the longest off-critical path was small, the supply voltage scaling, and hence, the power reduction were limited. Finally, using the hybrid structure to improve the effectiveness of the adaptive clock stretching operation has been investigated.

**IV. Proposed CSKA Structure**

As per the discussion it is concluded that by reducing the delay of the skip logic, one may lower the propagation delay of the CSKA significantly. Hence, in this paper, we present a modified CSKA structure that reduces this delay.

**General Description of the Proposed Structure:**

The structure is based on combining the concatenation and the incrementation schemes with the Conv-CSKA structure, and hence, is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates. The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented.

![Fig 2: Proposed CI – CSKA structure](image)

Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one.
Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths). Now, we describe the internal structure of the proposed CI-CSKA shown in below Fig. in more detail. The adder contains two N bits inputs, A and B, and Q stages.

The incrementation block uses the intermediate results generated by the RCA block and the carry output of the previous stage to calculate the final summation of the stage. The internal structure of the incrementation block, which contains a chain of half-adders (HAs), is shown in above Fig. In addition, note that, to reduce the delay considerably, for computing the carry output of the stage, the carry output of the incrementation block is not used. The skip logic determines the carry output of the jth stage ($C_{O,j}$) based on the intermediate results of the jth stage and the carry output of the previous stage ($C_{O,j-1}$) as well as the carry output of the corresponding RCA block ($C_j$). When determining $C_{O,j}$, these cases may be encountered. When $C_j$ is equal to one, $C_{O,j}$ will be one. On the other hand, when $C_j$ is equal to zero, if the product of the intermediate results is one (zero), the value of $C_{O,j}$ will be the same as $C_{O,j-1}$ (zero).

The reason for using both AOI and OAI compound gates as the skip logics is the inverting functions of these gates in standard cell libraries. This way the need for an inverter gate, which increases the power consumption and delay, is eliminated. An AOI is used as the skip logic, the next skip logic should use OAI gate. In addition, another point to mention is that the use of the proposed skipping structure in the Conv-CSKA structure increases the delay of the critical path considerably.

This originates from the fact that, in the Conv-CSKA, the skip logic (AOI or OAI compound gates) is not able to bypass the zero carry input until the zero carry input propagates from the corresponding RCA block. To solve this problem, in the proposed structure, we have used an RCA block with a carry input of zero (using the concatenation approach). This way, since the RCA block of the stage does not need to wait for the carry output of the previous stage, the output carries of the blocks are calculated in parallel.

**Proposed Hybrid Variable Latency CSKA Structure:**

The basic idea behind using VSS CSKA structures was based on almost balancing the delays of paths such that the delay of the critical path is minimized compared with that of the FSS structure. This deprives us from having the opportunity of using the slack time for the supply voltage scaling. To provide the variable latency feature for the VSS CSKA structure, we replace some of the middle stages in our proposed structure with a PPA modified in this paper. It should be noted that since the Conv-CSKA structure has a lower speed than that of the proposed one, in this section, we do not consider the conventional structure. The proposed hybrid variable latency CSKA structure where an Mp-bit modified PPA is used for the pth stage (nucleus stage). Since
the nucleus stage, which has the largest size (and delay) among the stages, is present in both SLP1 and SLP2, replacing it by the PPA reduces the delay of the longest.

Thus, the use of the fast PPA helps increasing the available slack time in the variable latency structure. It should be mentioned that since the input bits of the PPA block are used in the predictor block, this block becomes parts of both SLP1 and SLP2. In the proposed hybrid structure, the prefix network of the Brent–Kung adder is used for constructing the nucleus stage. One the advantages of the this adder compared with other prefix adders is that in this structure, using forward paths, the longest carry is calculated sooner compared with the intermediate carries, which are computed by backward paths. In addition, the fan-out of adder is less than other parallel adders, while the length of its wiring is smaller. Finally, it has a simple and regular layout.

V. Simulation Result

Design summary:

The written Verilog HDL Modules have successfully synthesized and simulated using Xilinx 14.5.
Simulation results:

VI. Conclusion

In this paper, a static CMOS CSKA structure called CI-CSKA was proposed, which exhibits a higher speed and lower energy consumption compared with those of the conventional one. The speed enhancement was achieved by modifying the structure through the concatenation and incrementation techniques. In addition, AOI and OAI compound gates were exploited for the carry skip logics. The efficiency of the proposed structure for both FSS and VSS was studied by comparing its power and delay with those of the Conv-CSKA, RCA, CIA, SQRT-CSLA, and KSA structures. The results revealed considerably lower PDP for the VSS implementation of the CI-CSKA structure over a wide range of voltage from super-threshold to near-threshold.

The results also suggested the CI-CSKA structure as a very good adder for the applications where both the speed and energy consumption are critical. In addition, a hybrid variable latency extension of the structure was proposed. It exploited a modified parallel adder structure at the middle stage for increasing the slack time, which provided us with the opportunity for lowering the energy consumption by reducing the supply voltage.

Extension Work:-

As an extension for this project we can implement the 64 bit adder using the same technique.

References