IMPROVE THE PERFORMANCE OF SHUNT ACTIVE POWER FILTERS WITH CONTROL STRATEGY OF ROBUST DC-LINK VOLTAGE

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ABSTRACT- In this paper, a Shunt active power filters (SAPFs) is developed without considering any harmonic detection schemes which are content with the sudden load different. The proposes system content with a robust control strategy to decreases this disadvantage. Therefore in this strategy, the dc-link voltage have been regulated by using a hybrid control method with the combination of the standard proportional–integral PI and also a sliding-mode (SM) controllers. The SM scheme determines continuously about the gains of the PI controller which is depend up on the control loop error and its derivative. Therefore the chattering which is due to the SM scheme is decreases by the transition rule that fixes the controller gains when steady state condition is needed. Therefore this controller is known as the dual-sliding-mode-proportional–integral. Here the phase currents of the power grid which are indirectly regulated by using the double sequence controllers with two degrees of freedom, where the internal model principle is implemented for avoid reference frame transformation. In this the proposed control strategy ensures zero steady-state error and also increases the performance during the hard transients such as load different. Simulation results demonstrate the performance of the proposed control scheme.

Index Terms—Adaptive control strategy, harmonic compensation, power factor correction, shunt active power filter (SAPF).

I. INTRODUCTION

Nowadays, the implementation of the power converters as embedded devices in house, commercial, or industrial electronic-based appliances has deteriorated the ability quality of the mains[1-2]. Those nonlinear hundreds generate current harmonics and reactive power that lead to voltage drops on the availability network electric resistance and should induce unbalance operative conditions.

SAPFs are mostly used for the compensation of harmonics, reactive power, negative sequences, and/or sparkles [5] – [7]. The traditional management schemes applied to SAPF square measure HEBSs as a result of their effectiveness depends on however quickly and accurately the harmonic elements of the nonlinear hundreds square measure known [6]. The SAPF may be additionally enforced while not the utilization of the load harmonic extractors. During this case, the harmonic compensating term is obtained from the system active power balance [7]. The management systems of SAPF enforced supported HEBS or BEBS ideas square measure typically accomplished by a cascade strategy composed by associate degree inner management loop for regulation the filter part currents (HEBS) or grid part currents (BEBS) associate degreed an outer management loop to line the dc-link voltage. The effectiveness of each solution depends on the performance of the management loops. Within the case of HEBS, the clink controller regulates the dc electrical device voltage at the appropriate level to attain the compensation objectives.

Now a days, a distinct approach of associate degree accommodative management strategy applied for SAP F victimization the BEBS methodology has been planned for compensating the harmonic distortion, reactive power, and unbalanced load [10]. During this SAPF, the present management theme is enforced by associate degree accommodative pole placement management, integrated with a variable structure theme (VS-APPC). The most advantage of the planned management strategy refers to the reduction of SAPF complexness of implementation, leading to reduced prices (because it's not necessary to own load and filter part current measurements, so reducing the amount of current sensors), while not reduction of its compensation effectiveness.

In this paper proposes a sturdy management strategy to boost BEBS power filters throughout severe load changes. During this approach, the dc-link voltage is regulated by a hybrid management strategy composed by the association of a regular PI and SM controllers[3].

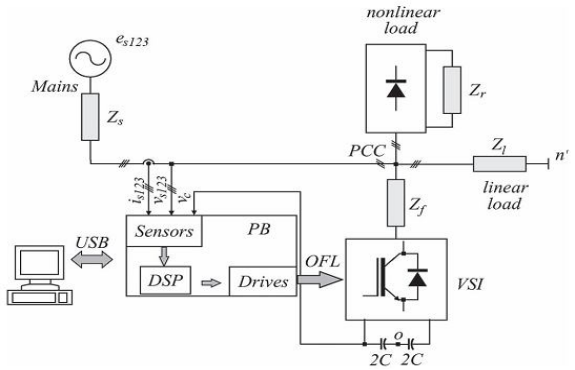

Fig. 1. Basic diagram of the proposed SAPF system.

The SM theme endlessly determines the gains of the PI supported the control loop error and its by-product. The chattering as a result of the SM theme is reduced by a transition rule that fixes the controller gains once system steady state is reached. The grid part currents square measure indirectly regulated by DSCs with 2 degrees of freedom, wherever the IMP is used to avoid reference system transformation

SYSTEM DESCRIPTION AND MODELING

Fig. 1 presents the topology of SAPF is present in this paper. It comprises a three-phase grid source es123 with its internal impedance (Zs = rs + sls) that feeds a three-phase load bank consisting of parallel association of a no controlled rectifier and a three-phase linear load (Zl = rl + sll).

A. SAPF Grid-Tied Power Converter Modeling

The model of the SAPF grid-tied power converter considering the interaction of the grid impedances to both the system. Based on this study, the system in Fig. 1 can be described by the per phase equivalent circuit presented in Fig. 2.

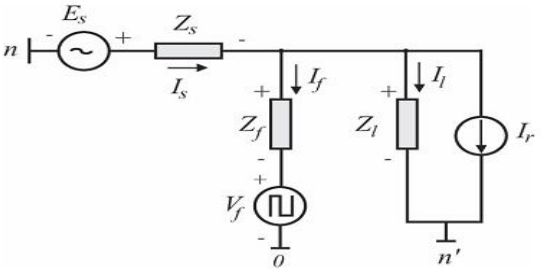

Fig. 2. Equivalent circuit of a SAPF system

From the equivalent circuit shown in Fig. 2, the transfer function representing the dynamic behavior of power grid currents can be given by

$$G_c(s) = \frac{I^{sf}_{sdq}(s)}{V^{s}_{fdq}(s)} \approx -\frac{b_s}{s+a_s} \qquad (1)$$

Where b s = 1/ (lf + ls), and as = (rf + rs)/ (lf + ls). In this model, parameters as and bs may vary as a function of either the random behavior of nonlinear load or the grid impedances. Further details on the system modeling could be found in [17]. The SAP F in Fig. 1 employs aluminum electrolytic capacitors in its dc link to ensure a constant dc voltage vC.

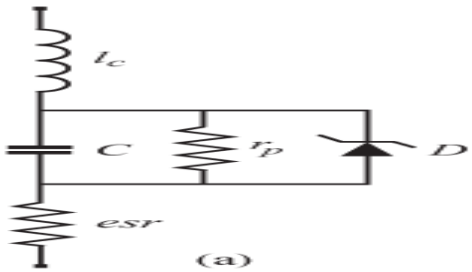

Fig. 3. Equivalent circuit of the electrolytic capacitor. (a) Manufacturer model.

The model chosen in this paper is shown in Fig. 3(a). It is the same used by manufacturers and also it is described by parameters easily identifiable. Thus, the equivalent circuit of the capacitor can be reduced to the one shown in Fig. 3(b).

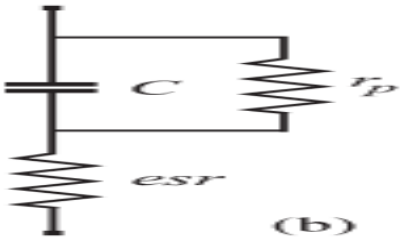

Fig. 3. Equivalent circuit of the electrolytic capacitor. (b) Simplified model.

Based on this equivalent circuit, the dynamic model of the electrolytic capacitor can be given by

$$\frac{V_C(s)}{I^e_{sd}(s)} = \frac{esr\left(s+\frac{1}{r_pC}+\frac{1}{esrC}\right)}{s+\frac{1}{r_pC}} \qquad (2)$$

The transfer function represented by (2) has a pole that depends on the values of C and rp and a zero depending on the values of C, rp, and esr. Considering a reasonable case where rp,esr, it is possible to simplify the model given by (2), neglecting the value of esr. In this case, the resulting transfer function is given by

$$G_v(s) = \frac{V_C(s)}{I^e_{sd}(s)} = \frac{\frac{1}{C}}{s+\frac{1}{r_pc}} = \frac{b_c}{s+a_c} \qquad (3)$$

Where b c = 1/C, and ac = 1/ (rpC). The dynamic behavior of both models varies depending on C, rp, and esr, which in turn vary as a function of frequency, voltage, and temperature.

III. CONTROL SCHEME

Fig. 4 presents the block diagram of the proposed control scheme for the SAP F based on the methodology. It is done by generating the reference current iesd ∗, which determines the system active power component. The phase angle of the power grid voltage vector θs is determined by using a P LL.

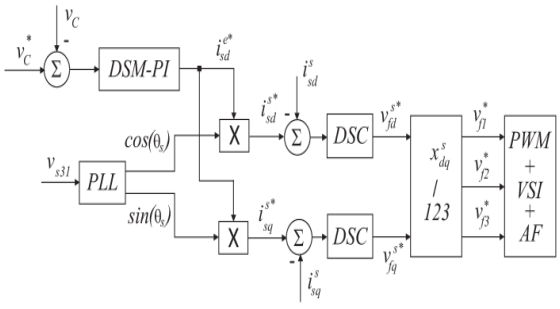

Fig. 4. Block diagram of the proposed control strategy. *Xedq* denotes voltage vector reference frame variables, whereas *xs dq* denotes stationary reference frame variables.

A. Grid Currents Control Strategy

The control strategy employed in this paper for regulating the grid currents (see block DSC in Fig. 4) is based on the double sequence control scheme, which employs one controller for the positive sequence and another for the negative sequence [32]. Generically, the state space model of the DSC can be represented by

$$\frac{dx^s_{1dqi}}{dt} = 2k_{ii}\varepsilon^s_{idq} + x^s_{2dqi} \quad (4)$$

$$\frac{dx^s_{2dqi}}{dt} = -\omega_s^2 x^s_{1dqi} \quad (5)$$

$$v^{s*}_{fdq} = x^s_{1dqi} + 2k_{pi}\varepsilon^s_{idq} \quad (6)$$

Where k pi and kii are the controller gains and ωs is the fundamental frequency of the power grid. The transfer function of the current controller on the stationary reference frame can be given by

$$C_c(s) = \frac{2k_{pi}s^2+2k_{iiS}+2k_{pi}\omega_s^2}{s^2+\omega_s^2} \quad (7)$$

The design of the DSC is achieved by using the zero pole cancelation method. Therefore, considering that as can be associated to the current controller gains kpi and kii as

$$a_s \approx \frac{k_{ii}}{k_{pi}} \quad (8)$$

The desired band pass frequency of the DSC can be determined as ω c = bskpi. Thus, it is possible to determine the controller gains as a function of as and bs, which results in

$$k_{pi} = \frac{\omega_c}{b_s} \quad (9)$$

$$k_{ii} = \frac{a_s\omega_c}{b_s} \quad (10)$$

Different design methodologies can be employed for calculating the current controller gains. Here, the proposed design approach achieves a good performance in the current control loop.

B. DC-Link Voltage Controller

The proposed control scheme for the dc link is implemented by a nonstandard robust SM − P I, which is implemented by a proportional–integral (P I) controller in which its controller gains are calculated by using the SMC approach based on the sliding surface composed by the control loop error and its derivative.

1) SM −P I Control Scheme:

Consider the dynamic model of the dc link of the SAP F described by (3) with the value of esr neglected. Admitting that the SM − P I controller transfer function can be written as

$$C_v(s) = \frac{\tilde{k}_p s+\tilde{k}_i}{s} \quad (11)$$

Controller gains KP and ki are determined by SMC theory. The closed-loop dynamics of the dc-link voltage can be described as follows:

$$V_c(s) = \frac{b_c\tilde{k}_p(s+\tilde{k}_i/\tilde{k}_p)}{s^2+(a_c+b_c\tilde{k}_p)s+b_c\tilde{k}_i}V_c^*(s) \quad (12)$$

During the transient state, the gain KP switches between kav p and 2kp + and KP av − 2kp +. Upon reaching the steady state, kp is kept constant at kp av. A similar statement applies to ki. Stability of the dc link is assured whenever

$$a_c + b_c\tilde{k}_p > o \quad (13)$$

$$b_c\tilde{k}_i > o \quad (14)$$

By using a suitable design procedure, these conditions can be easily fulfilled. Define a sliding surface described by

$$\sigma = ce_v + \dot{e}_v \quad (15)$$

Where e v = vc ∗ − vc, e ˙v is its derivative, and c is a positive constant. To prove the stability of the proposed SM − P I at the origin (σ = 0), let the Lyapunov candidate be

$$V(e_v) = \frac{1}{2}e_v^2 \quad (16)$$

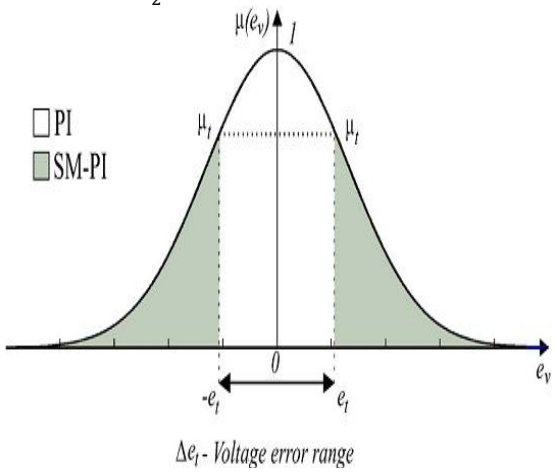

Fig. 5. Graph of the transition criterion μ.

Therefore, its time derivative can be expressed as

$$\dot{V}(e_v) = e_v\dot{e}_v = e_v(-ce_v) = -ce^2{}_v < 0 \quad (17)$$

Since constant c is positive, the proposed control is asymptotically stable. Based on these stability restrictions, the controller gains can be determined by using the following switching laws:

$$\tilde{k}_p = \left[(1+sgn(\sigma))k_p^+ - (1-sgn(\sigma))k_p^-\right] + k_p^{av} \quad (18)$$

$$\tilde{k}_i = \left[(1+sgn(\sigma))k_i^+ - (1-sgn(\sigma))k_i^-\right] + k_i^{av} \quad (19)$$

Where k^+_p , $k_p{}^-$, $k_i{}^+$, $k_i{}^-$, $k_p{}^{av}$, and $k_i{}^{av}$ are positive constants determined as a function of the desired system performance (these gains can be obtained by using a standard P I design methodology, e.g., root locus). The mathematical function sgn(σ) returns the values 1 for σ > 0 or −1 for σ < 0.

2) DSM−PI Control Scheme: The SM−PI controller has a good performance during the transient state but has an undesired side effect when the steady state is reached. It can be obtained by employing a transition rule in the controller structure. For this, consider a Gaussian function defined as

$$\mu(e_v) = e^{-\frac{e_v^2}{\lambda}} \quad (20)$$

where μ is the decision variable to select between the switching and fixed controllers, ev is the dc-link voltage error, and λ is the parameter of the Gaussian function.

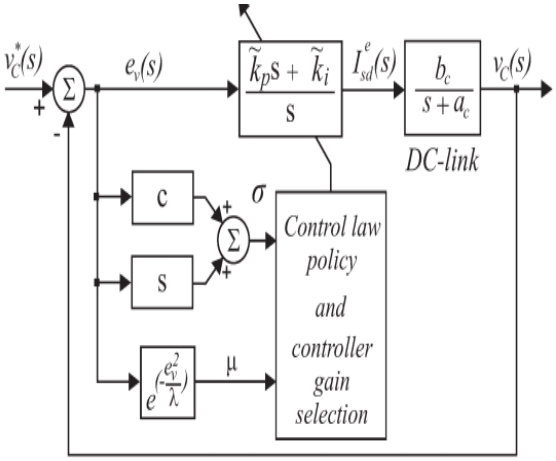

Fig. 6. Block diagram of the DSM − P I control scheme. The kp and ki gains updating policy is as follows: for μ (ev) < μt, the gains change according to (23) and (24), and for μ (ev) μt, the gains are kept constant.

The block diagram of the proposed DSM − P I controller is shown in Fig. 6.

3) Design Criteria of the DSM−PI: The design criterion employed in this paper is based in the pole assignment that requires the solution of the Diophantine equation. Thus, consider the transfer functions of dc link [see (3)] and the voltage regulator DSM − P I [see (11)] can be written in terms of polynomials.

$$G_v(s) = \frac{Z(s)}{R(s)} \quad (21)$$

$$C_v(v) = \frac{P(s)}{L(s)} \quad (22)$$

where Z(s) = bc, R(s) = s + ac, P (s) = kps + ki, and L(s) = s. Then, the transfer function of the dc-link control loop will be given by

$$T_{et}(s) = \frac{Z(s)P(s)}{Z(s)P(s)+R(s)L(s)} \quad (23)$$

whose characteristic equation is

$$Z(s)P(s) + R(s)L(s) = 0 \quad (24)$$

The design objective is to find suitable polynomials $P(s)$ and $L(s)$ such that

$$Z(s)P(s) + R(s)L(s) = A^{\eta*}(s) \quad (25)$$

Where Aη∗(s) is a desired harmonic Hurwitz polynomial, and superscript η ∈ {fs (fast), av (average), sl (slow)} refers to the performance criteria employed for determining desired polynomials.

IV. SIMULATION EVALUATION OF THE PROPOSED SAPF

Fig.8 depicts the simulation outcome comparing both controllers following a reference ramp. Such a ramp waveform has a slope of 347 V/s.

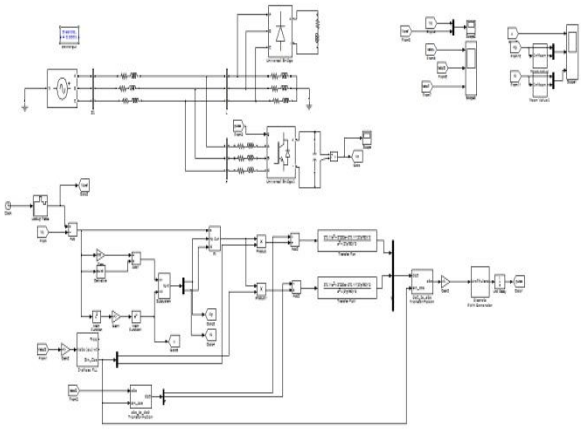

Fig.7. Block diagram of simulation.

In Fig.8. that the performance of the proposed converter is smoother and the response time is smaller; the overshoot values of the proposed and conventional converters are given respectively by 0.53% and 4.37%.

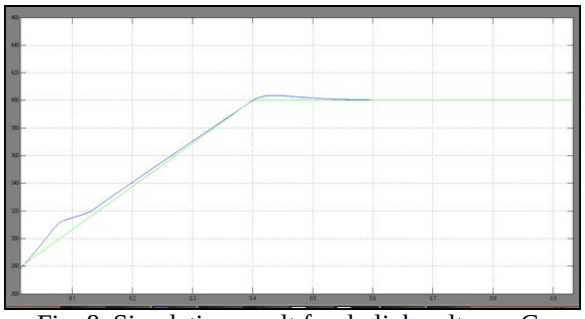

Fig. 8. Simulation result for dc-link voltage vC during startup.

Although the comparison shown in Fig. 8 brings up the benefits of the DSM−P I strategy, additional tests have been considered to highlight its advantage under operating regimes.

Fig.9. Simulation result for dc-link voltage vC during step transient of its reference voltage with both step-up and step-down variations.

For instance, Fig. 9 presents a comparison for both controllers for variations of the dc-link reference voltage. A zoom of the transient at t = 5 s is presented in Fig. 10, whereas Fig. 11 shows a zoom of the step-down transient at t = 9 s.

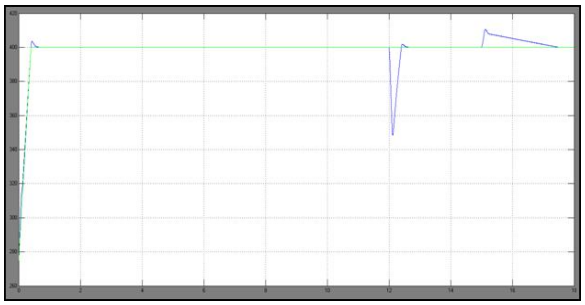

Fig. 11. Simulation result for dc-link voltage (vc) during load transients.

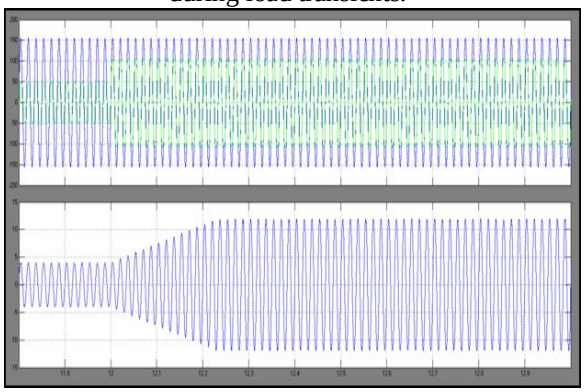

Fig. 12. Simulation result during load transients (a) for dc-link voltage vc, (b) for source voltage vs1 and the load current il1 multiplied by 10 times, and (c) for source current is1.

On the other hand, Figs. 11–13 show a typical type and ever-present transient in active power filter applications, i.e., transitory of load power. Two types of variations are considered; the first one (see Fig. 12) at t = 12 s shows the load power increase with an additional three-phase resistor (30 Ω) connected in parallel with the arrangement of linear and nonlinear loads.

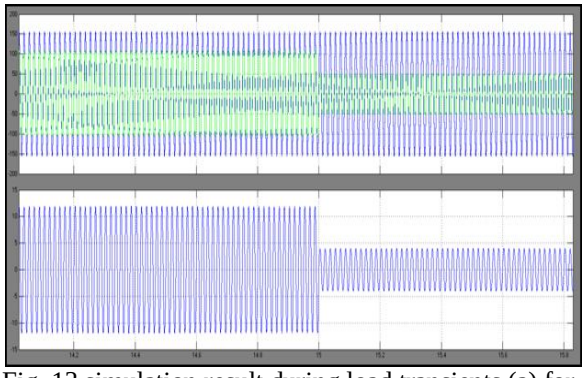

Fig. 13.simulation result during load transients (a) for dc-link voltage vc, (b) for source voltage vs1 and the load current il1 multiplied by 10 times (c) for source current is1.

The DSM − P I controller also performs better than the conventional approach with load power reduction (see Fig. 13), as observed at t = 15 s. Such a transient was obtained by disconnecting the resistive load.

Fig. 14. Simulation result for function μ used for commutation between the controllers P I and DSM − PI.

CONCLUSION

The control system of the proposed method which is approach for betterment of the performance of SAPF without any load current measurements. Therefore in this control system it is approach to the dc-link voltage which is regulated by using a dual control method developed by the proportional–integral (PI) controller with the calculation of gains by using an SMC approach. The chattering due to the SM can be mitigated by using a transition rule in the controller structure. The theoretical analysis of the SM −PI are introduced, along with the stability which are proven and it is presented in the paper. Moreover, the transition scheme that results in DSM−PI was also discussed. Moreover the control strategy and it's the performance of the dc-link control loop during the load different is improved. The phase currents of the power grid which are indirectly regulated by using the two independent controllers (DSCs), in which the IMP is implemented to avoid reference frame transformations. In this verification there are few significant gains in the SAPF which are depend upon the BEBS since the current control strategy is simpler and the filter control strategy is developed to decreases the current sensors. Therefore the simulation result shown the proposed control strategy during the load different it will improve the system reactive power compensation and harmonic mitigation.

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