THIRTEEN LEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES USING DIFFERENT PWM TECHNIQUES

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ABSTRACT- In this paper analysis and design of three phase 13-level inverter configuration is proposed with less total harmonic distortion (THD). Conventional bipolar inverters produce alternating staircase waveforms with higher harmonics. Thus, the multilevel inverters (MLI) were developed. As compared to conventional inverter topologies like diode clamped and capacitor clamped inverters, the cascaded multilevel inverter has lesser harmonics as well as lower switching stress. The cascaded topology has more number of power switches leading to greater heat losses, larger size, higher cost and more gate drive circuitry. IPD, APD, CO and VF PWM techniques were used to produce switching pulses. A comparison between four different types of pulse width modulation (PWM)techniques, namely, In-phase disposition (IPD), Anti-phase disposition (APD), Carrier Overlap (CO) and Variable Frequency (VF) PWM methods, has been analyzed in this paper. An LC filter has been designed to reduce the harmonics. The proposed configuration contains less number of switches and produces lesser harmonics in the output voltage than the cascaded topology. As the number increases the synchronized output waveform has more steps, which produces a staircase waveform that approaches a desired waveform. To analyze the best PWM method that provides minimum THD in the output voltage the results have been verified by using simulation results.

I.INTRODUCTION

In recent days MLI has drawn large interest in high power industry. They present a latest set of aspects to facilitate and utilized in reactive power compensation. The unique arrangement of multilevel voltage source inverters allow them to achieve high voltages with the low harmonics not including the utilization of transformers or series connected synchronized switching devices. From renewable energy sources like photovoltaic array and wind energy power electronic devices play a major role in the conversion and control of electric power, especially to extract power. Conversion of DC to AC power can be done with the help of inverters (single phase or three phases). The multi level inverters (MLI) were developed because conventional bipolar inverters produce alternating staircase waveforms with higher harmonics. Also as more steps are added to the waveform the harmonic distortion of the output wave decreases approaching zero as the number of levels increases. The cascaded H-bridge (CHB) configuration has lesser number of components as compared to the conventional diode clamped or capacitor clamped inverters.

Multilevel inverters can operate at both fundamental frequency and high switching frequency PWM. It should be noted that lower switching frequency means lower switching loss and higher efficiency.

To produce a sine waveform the staircase inverter output a passive series LC filter is designed. Due to the inverter switching the purpose of the output LC filter is attenuating voltage ripples .A three phase multilevel inverter is obtained by interconnecting three single phase inverters to a star connected pure resistive load with a common earth point. Therefore, this circuit offers lesser gate control circuitry, lesser cost, lesser heating, more ease of installation and lesser electromagnetic interference. Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped, flying capacitor or multi cell, cascaded H-bridge, and modified H-bridge multilevel. This paper recounts the development of one novel modified H-bridge single-phase multilevel inverter that has one diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique. the comparison of the number of components between different topologies as shown in Table. I.

TABLE. I:
NUMBER OF COMPONENTS PER PHASE FOR DIFFERENT I3-LEVEL INVERTER TOPOLOGIES

Sl. No.	Configuration	Number of switches per phase	Number of conducting switches per phase
1	Diode Clamped	24	5
2	Capacitor Clamped	24	5
3	Cascaded H-Bridge	24	12
4	Eight switch type	10	5

II.PROPOSED TOPOLOGY AND ITS OPERATION

The proposed three-phase thirteen-level inverter was developed from the multi-level inverter. This H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, for inverters of the same number of levels. Proper switching of the inverter can produce thirteen output-voltage levels (Vdc, 2Vdc, 3Vdc, 4Vdc, 5Vdc, 6Vdc, 0, -6Vdc, -5Vdc, -4Vdc, -3Vdc, -2Vdc,-Vdc) from the dc supply voltage

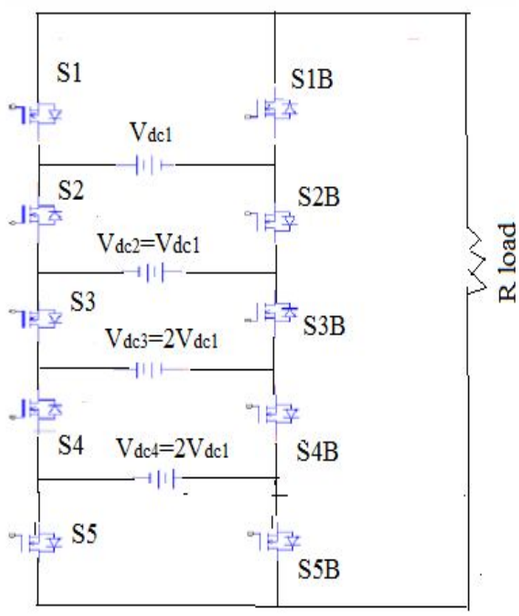
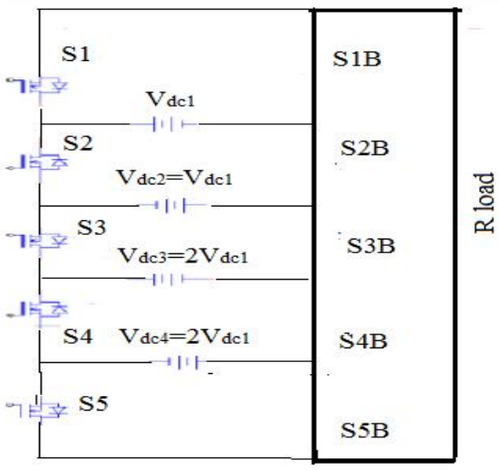


Fig.1. Proposed configuration for single phase multilevel inverter operation

TABLE.2:
SWITCHING STATES IN I3-LEVEL INVERTER

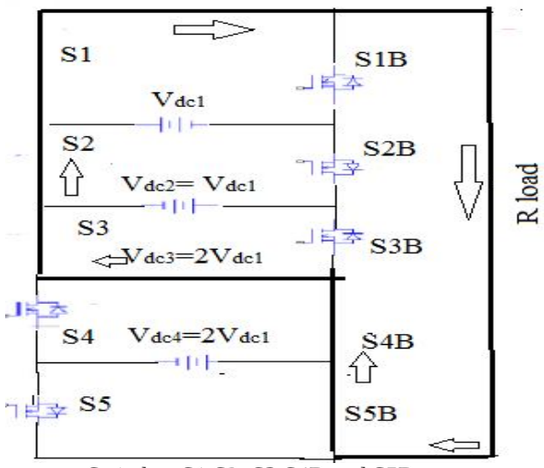
Output Voltage	S1	S2	S3	S4	S5	S1B	S2B	S3B	S4B	S5B
$+6V_{dc}$	1	0	1	0	1	0	1	0	1	0
$+5V_{dc}$	0	0	1	0	1	1	1	0	1	0
$+4V_{dc}$	1	1	1	0	1	0	0	0	1	0
$+3V_{dc}$	1	0	0	0	1	0	1	1	1	0
$+2V_{dc}$	1	1	1	0	0	0	0	0	1	1
V_{dc}	1	0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	1	1	1	1	1
$-V_{dc}$	0	1	1	1	1	1	0	0	0	0
$-2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$-3V_{dc}$	0	1	1	1	0	1	0	0	0	1
$-4V_{dc}$	0	0	0	1	0	1	1	1	0	1
$-5V_{dc}$	1	1	0	1	0	0	0	1	0	1
$-6V_{dc}$	0	1	0	1	0	1	0	1	0	1
0	1	1	1	1	1	0	0	0	0	0

MODE 1(0 VOLTAGE LEVEL)



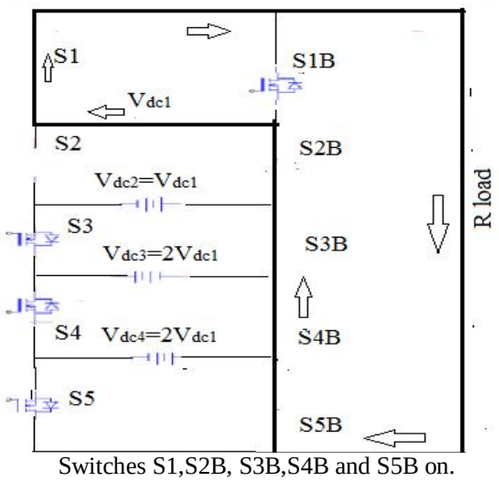
Switches S1B,S2B, S3B,S4B and S5B on

MODE 3(VOLTAGE LEVEL: +2VDC)



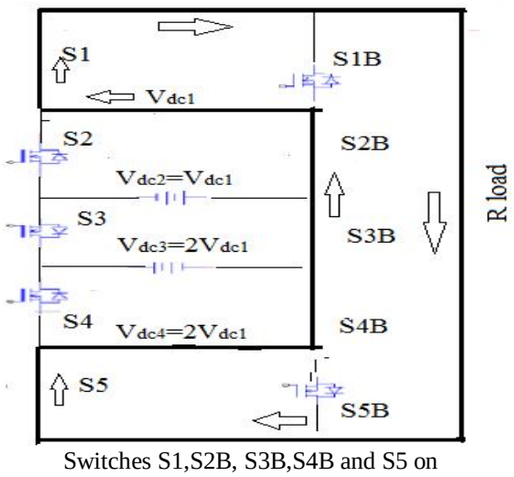
Switches S1,S2, S3,S4B and S5B on

MODE 2(VOLTAGE LEVEL: +VDC)



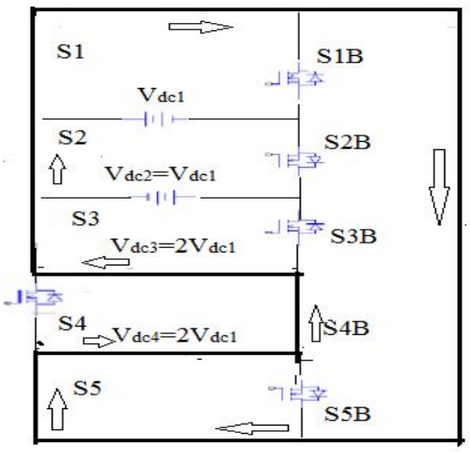
Switches S1,S2B, S3B,S4B and S5B on.

MODE 4(VOLTAGE LEVEL: +3VDC)



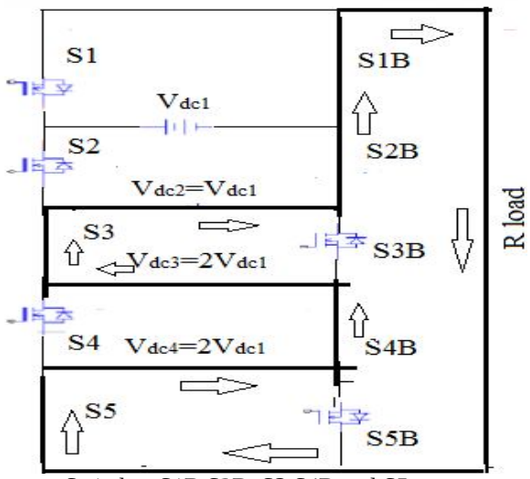
Switches S1,S2B, S3B,S4B and S5 on

MODE 5(VOLTAGE LEVEL:+4VDC)



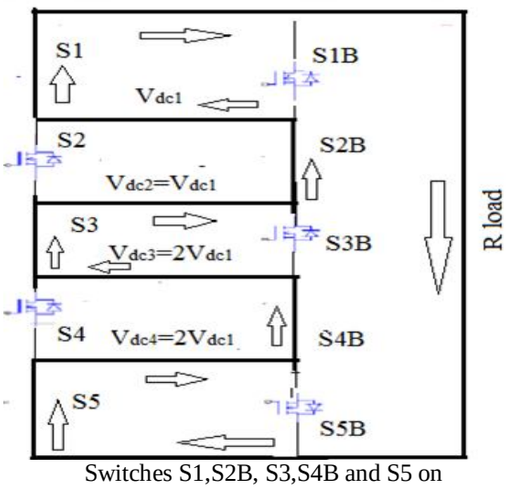
Switches S1,S2, S3,S4B and S5 on

MODE 6(VOLTAGE LEVEL:+5VDC)



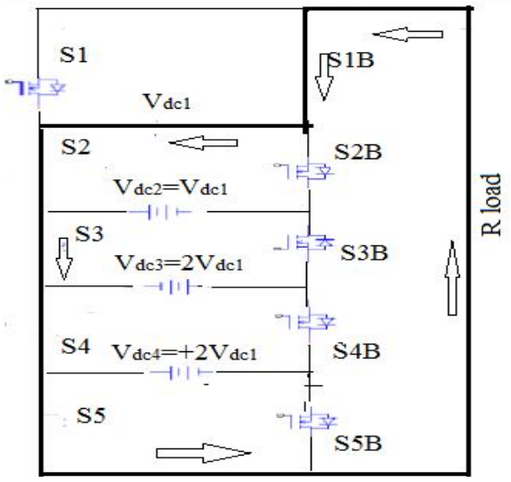
Switches S1B,S2B, S3,S4B and S5 on

MODE 7(VOLTAGE LEVEL: +6VDC)



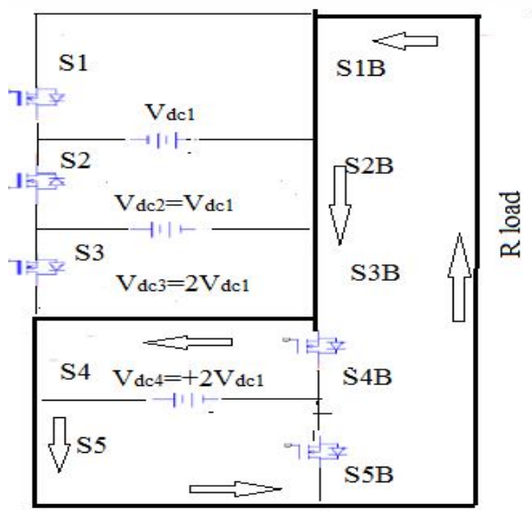
Switches S1,S2B, S3,S4B and S5 on

MODE 8(VOLTAGE LEVEL:-VDC)



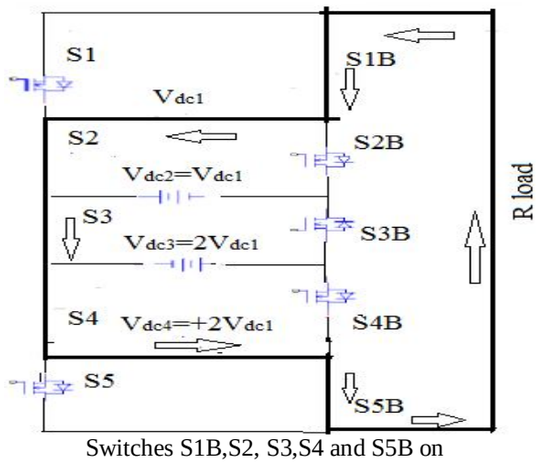
Switches S1B,S2, S3,S4 and S5 on

MODE 9(VOLTAGE LEVEL: -2VDC)



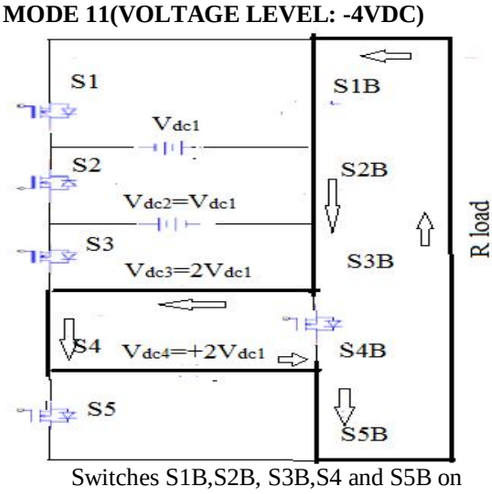
Switches S1B,S2B, S3B,S4 and S5 on

MODE 10(VOLTAGE LEVEL: -3VDC)



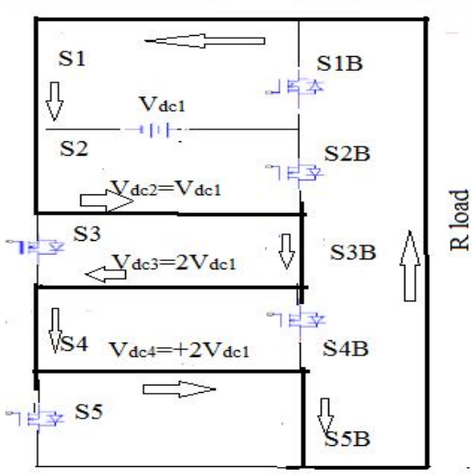
Switches S1B,S2, S3,S4 and S5B on

MODE 11(VOLTAGE LEVEL: -4VDC)



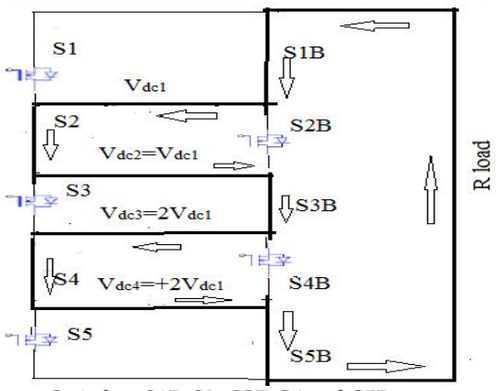
Switches S1B,S2B, S3B,S4 and S5B on

MODE 12(VOLTAGE LEVEL: -5VDC)



Switches S1,S2, S3B,S4 and S5B on

MODE 13(VOLTAGE LEVEL: -6VDC)



Switches S1B,S2, S3B,S4 and S5B on

Fig.2. States corresponding to each Output voltage level

III.MODULATION SCHEMES

In this paper pwm technique is used to generate the thirteen level output voltage.. It is used to control the frequency and harmonics of the output voltage of the inverter, so we must select the most appropriate PWM technique. To the power switches the sinusoidal PWM (SPWM) method has been applied, in which a reference sinusoidal wave of fundamental frequency is compared to high frequency carrier wave(s).

Based on the PWM technique the level, frequency or amplitude of the multiple carrier signals are varied. For comparison the modulation indices are kept same in all the methods. Amplitude modulation index is the ratio of the amplitude of the reference sine wave to the amplitude of the carrier waves. Amplitude modulation index rna and frequency modulation index mr are given by (1)and (2) respectively.

$$m_a = A_m / A_c \quad (1)$$

$$m_f = f_c / f_m \quad (2)$$

The PWM techniques discussed in this paper are In Phase Disposition (lPD) type level shift pulse width modulation (LS-PWM), Anti-Phase Disposition (APD) PWM, Carrier Overlap (CO) PWM and Variable Frequency (VF)PWM. In all the PWM techniques, 'N' number of carrier signals are used to obtain 2N+ 1 voltage levels. By using simulation results The RMS value of the fundamental component of the output voltage and the total harmonic distortion (THD) are observed.

A. In-Phase Disposition Level-Shift PWM(IPD-LSPWM) Method:

In this PWM technique the carrier signals are level shifted. They have the same amplitude of 1 V and a frequency of 10kHz. At fundamental frequency the level shifted carrier signals are compared with a diode bridge rectified reference sine wave which is illustrated in Fig.4. In order to obtain a three phase inverter, the sine wave is phase shifted by 120°.The different levels of the output wave is detected and to trigger each switch in the inverter decoded to produce the pulses required.

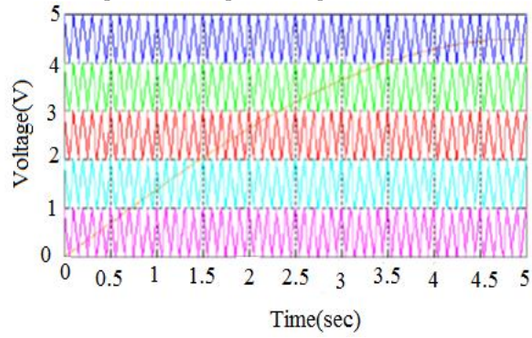


Fig 3.Reference Sine wave and Carrier waves for IPD-LSPWM at m_a=0.9 and m_f=200

B. Anti-Phase Disposition Level-Shift PWM(APD-LSPWM) Method:

As shown in Fig.5 to produce required gate pulses the carrier signals are compared with the reference sine wave (which is at fundamental frequency). Each carrier signal is out of phase with neighboring carrier signals by 180° and have the same amplitude and frequency

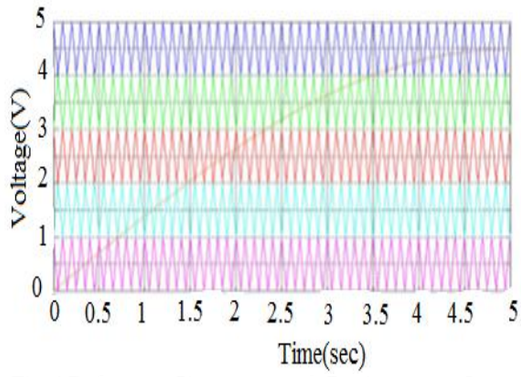


Fig 4.Reference Sine wave and Carrier waves J or APD-LSPWM at m_a=0.9 and m_r=200

C. Variable Frequency PWM (VF-PWM) Method:

To produce required switching pulses they are compared with the reference sine wave with fundamental frequency. All the level-shifted carrier waves have the same amplitude as shown in Fig.6,. The lowermost carrier wave has very high frequency, 10kHz followed by 8kHz, 6kHz, 4kHz and the uppermost carrier signal has lowest frequency, 2kHz.

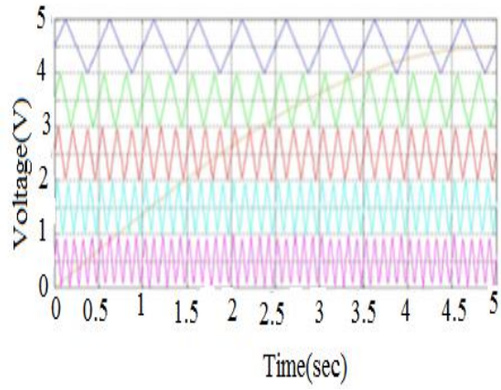


Fig 5.Reference Sine wave and Carrier waves J or VF-PWM at ma=O.9

D. Carrier Overlap PWM (CO-PWM) Method:

To produce the gate pulses this strategy utilizes level shifted carrier waves of the same frequency and amplitude. They are inphase with each other and also overlap each other.

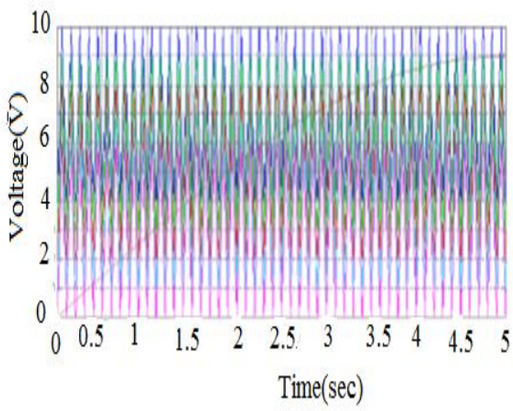


Fig 6.Reference Sine wave and Carrier waves J or COPWM method at m_a=0.9 and m_J=200.

IV.SIMULATION RESULTS & DISCUSSION

MATLAB SIMULINK simulated the proposed configuration before it was physically implemented. The same amplitude with offset of seven carrier signal is compared with the sinusoidal reference signal and the PWM signal is generated. At the same amplitude and frequency modulation various PWM techniques are applied to the proposed three phase inverter topology using MATLAB/ Simulink.

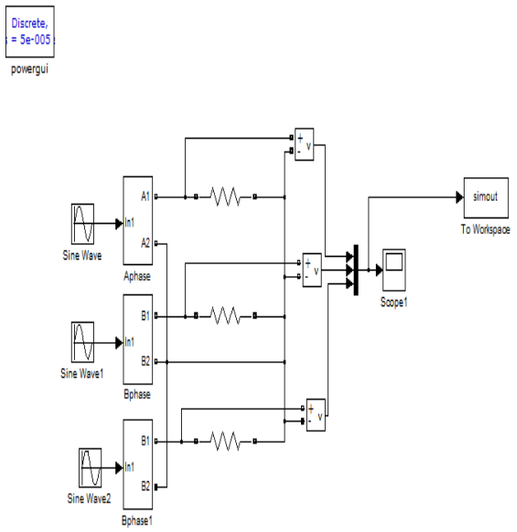


Fig 7. Block diagram of simulation

Using the Fast Fourier Transform(FFT) block a comparative study has been made between the RMS values of fundamental value of the output voltage and the total harmonic distortion for a single phase. The circuit parameters used are:
fc= 10kHz; fm= 50Hz; Am= 4.5V; Af= 5V.
Star connected resistance load (R = 50Ω)

The fundamental value of output voltage is higher and the THD is lesser in the IPD type LSPWM than the APD type. The carrier waves are in phase with each other in the IPD type, resulting in less complex circuitry.

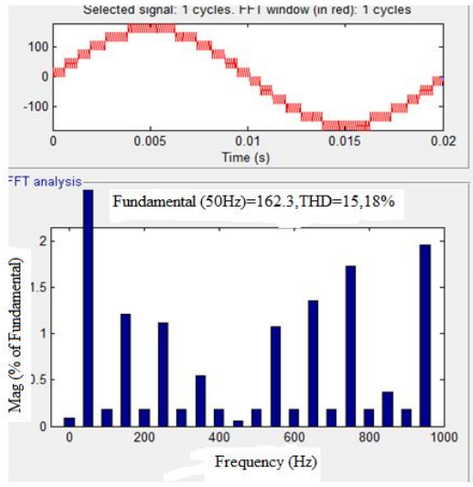


Fig 8. Output voltage waveform & FFT Analysis of the harmonic spectrum for three phase 13 level inverter using IPDLSPWM technique.

By using a suitable microcontroller kit The size and cost of the circuit can be reduced by opting for digital pulse generation. This method produces pulses that overlap each other. The carrier waves have larger amplitudes than other PWM techniques Hence, the resultant voltage waveform has very high THD, which is not close to the sine wave.Different carrier frequencies are used in this method, resulting in utilization of more analog components and large circuitry.

Based on the THD of the output voltage the performance analysis of the three phase inverter is given in Table.3.VF-PWM technique was found to be providing minimum harmonics in the output voltage among the four types.

TABLE.3
VRMS (FUNDAMENTAL) AND THD OF OUTPUT VOLTAGE FORCHOSEN TOPOLOGY FOR DIFFERENT PWM TECHNIQUES

Sl.No.	PWM Technique	RMS Value of FUNDAMENTAL of Output Voltage(in Volts)	THD (in %)
1	IPD-LSPWM	162.3	15.18
2	APD-LSPWM	163.3	15.28
3	CO-PWM	158.7	12.83
4	VF-PWM	160.7	10.83

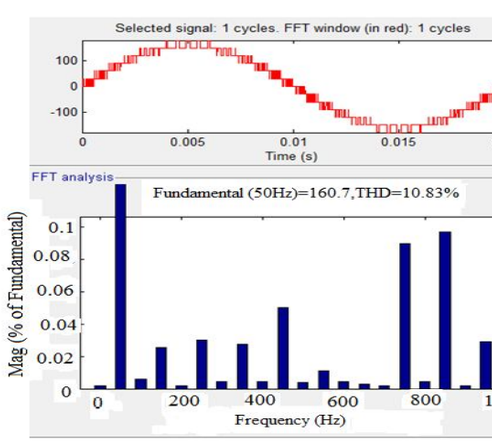


Fig 9.Output voltage waveform& FFT Analysis of the harmonic spectrum for three phase 13 level Inverter using VFPWM Technique.

V.OUTPUT AFTER USING AN LC FILTER

Various PWM methods are analyzed and compared. From the simulation results, it was found that VF-PWM provides minimum THD of 12.51 % in the inverter output voltage. This will be the best PWM technique for inverters witching because small inductance can be used in the LC filter placed in series to the inverter output to produce a rectified AC sine wave of low THD of 1.77%.

To produce a sinusoidal waveform with reduced THD An L-C filter is connected at the output of the inverter. To maintain the switching ripple current the L andC values are designed under the target value. The inductance value is thus given by:

$L \geq R_{L\text{-}max}/3\omega$ for single phase (3)

$L \geq 2*R_{L\text{-}max}/p(p^2\text{-}1)\omega$ for poly phase (4)

(Where p=number of phases and$\omega = 2\pi f$)

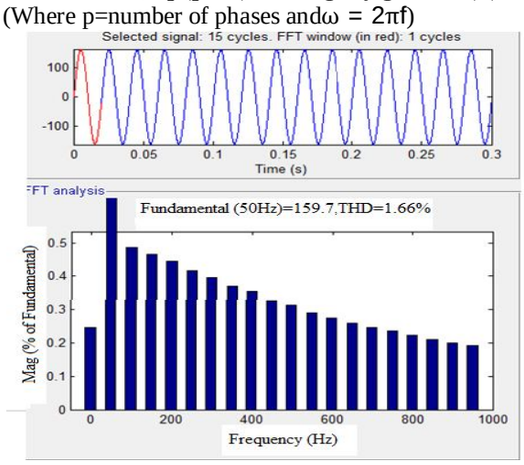


Fig 10.Sinusoidal output voltage waveform& FFT Analysis of the harmonic spectrum for three phase 13 level inverter using VF-PWM technique with series LC filter.

VI.CONCLUSION

This paper has presented a novel PWM switching scheme for the proposed multilevel inverter. The proposed configuration contains less number of switches and produces lesser harmonics in the output voltage than the cascaded topology. A comparison between four different types of pulse width modulation (PWM) techniques, namely, In-phase disposition (IPD), Anti-phase disposition (APD), Carrier Overlap (CO) and Variable Frequency (VF) PWM methods, has been analyzed in this paper. Multilevel inverters offer improved output waveforms and lower THD. From the simulation results, it was found that VF-PWM provides minimum THD of 10.83 % in the inverter output voltage. This will be the best PWM technique for inverters because small inductance can be used and also produce a rectified AC sine wave of low THD. The total harmonic distortion for each level is calculated and compared for resistive load. At different levels THD can be decreased by increasing number of levels which validates the proposed control strategy is proposed .

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