ENHANCING THE SPACE UTILIZATION OF FILE SYSTEM ON PCM STORAGES THROUGH MGBM

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ABSTRACT– ***PCM is rapidly developed as a promising candidate for next-generation storage class memory (SCM) because of its non-volatility, byte-addressability, and high access performance. In recent years, researchers have studied how to use PCM as main memory or hybrid main memory to improve the system performance and energy efficiency. Although some studies have explored the read/write asymmetry of PCM to further optimize the performance of PCM, using PCM as main memory suffers from the write endurance issue. As for the space utilization of file system designs, a number of previous studies proposed different management designs to improve the space utilization of file systems over block-based storage devices. However, to the best of our knowledge, little research has been done trying to optimize the space utilization of file systems by taking advantage of the nice features of PCM. In this paper we propose a multi-grained block management strategy to improve the space utilization of file systems over PCM-based storage systems with minimized space and management overheads.***

Keyword: Phase Change Memory, Block-based Storage

1. INTRODUCTION

A PCM cellular is collected of an access transistor and a storage resistor fabricated from a chalcogenide alloy. With the application of warmth, the alloy can be transitioned among bodily states with unique resistances, used to represent binary values. Via thermal induction, PCM cells can transition between a high electric resistance country (logical 0) and a low one (logical 1). PCM can interface with maximum CMOS peripheral circuitry used in DRAM. Unlike in DRAM, PCM's reads are non-adverse and cells can retain records for several years. On the drawback, PCM cells exhibit worse get entry to overall performance than DRAM. Regarding density, PCM has kind of the identical mobile length as DRAM. However, PCM permits manufacturing of multi-level cells (MLC), that can shop multiple (currently, 2 or 4) bits. Assuming the same cellular length for each technology, these MLCs hold 2x and 4x information than DRAM cells inside the equal location.

Currently, applications have higher necessities at the processor and reminiscence device. Over the past decades, the fast development of multi-middle technology has improved the parallelism and the

performance of the processors, which allows many threads or packages to run simultaneously. However, traditional memory systems fail to fulfill the wishes of fast I/O operations and huge ability. The overall performance gap among computation (e.g., the multi-center processors) and storage (e.g., DRAM) causes the performance degradation in the entire device. The advent of 20-nanometer semiconductor generation has been challenged with the aid of energy and scalability of the refresh operation in Dynamic Random Access Memory (DRAM) medium. For instance, Lefurgy mentioned 40% of the electricity consumption by using the main reminiscence in the IBM eServer servers. Non-volatile memory generation can update DRAM and build a big-capability and strength-efficient storage machine, inclusive of Phase Change Memory (PCM), Magnetic Random Access Memory (MRAM) and Resistive Random Access Memory (ReRAM). Among them, PCM is the maximum promising candidate for building predominant-reminiscence systems. Compared with DRAM generation, PCM shows asymmetrical examine/write latency. The latency of write operation is 4 ∼ 8 times longer than that of read operation, which incurs intense bank conflicts. The long write latency is much more likely to dam incoming reminiscence accesses to the equal financial institution. Bank conflicts, coupled with the write latency, drastically reduce reminiscence bandwidth utilization and might purpose cores to stall, leading to decrease gadget performance. In order to deal with this trouble, current research advocate an correct-and-tight electricity control method for the PCM gadget, which exploits modern distinction between writing bit 0 and bit 1 so as to leverage the excess unused power finances to serve more requests inside a bank. This approach has been applied into the practical PCM chips, which increase a multi-partition structure within each financial institution. The new chips show the superior feature that a examine operation is feasible to be served in a single partition even as write in every other partition. Thus, it presents a brand new manner to decorate device performance by using exploring partition-stage parallelism. Compared with banks which might be the smallest unbiased shape, the parallelism among walls has greater restrictions. For instance, two or more write operations are not allowed to be simultaneously carried out in specific partitions inside a bank for limited strength constraint. Therefore the partition-level parallelism is weaker than the bank-level one.

2. RELATED WORK

Katelin A. Bailey, Peter Hornyack, Luis Ceze, Steven D. Gribble and Henry M. Levy supplied the layout and implementation of Echo, a key-price storage machine explicitly designed for future garage-magnificence memory technologies. Echo is meant to provide the durability guarantees of block-storage structures while achieving the overall performance and scalability commensurate with present day key-price shops. Key to Echo's design is its -degree reminiscence structure and the use of image isolation for concurrency, consistency, and versioning. The easy measurements offered show the potentials of Echo's design to satisfy their goals.

M. K. Qureshi, V. Srinivasan, and J. A. Rivers proposed a novel hybrid PCM device that leveraged eDRAM to create a cache for the PCM memory that replaces the row buffer. This eliminates the need for a couple of reminiscence controllers and gives minor overall performance gains and large strength

enhancements. This scheme improves the elegance of PCM as a capacity most important reminiscence alternative. This offers outstanding possibility to retain strength-green reminiscence scaling into the future.

Phase Change Memory (PCM) is one of the leading applicants in emerging memory technologies. Unfortunately, PCM has higher latency than DRAM, which degrades machine overall performance. Prashant J. Nair, Chiachen Chou, Bipin Rajendran, Moinuddin K. Qureshi studied architectural techniques to improve the examiner latency of PCM via exploiting the inherent variant in resistance characteristics of PCM cells. Rather than traditional designs that try to conceal variability, they contend that PCM structures ought to be designed for embracing variability and designing for better-than-worst-case situations.

3. FRAMEWORK

A. System Overview

By utilizing the byte-addressability of PCM, the proposed strategy can manage blocks with multiple granularities to reduce the internal fragmentation of blocks that store small files or the tail data of files; in other words, smaller blocks are used for smaller files and larger blocks are allocated for larger files. Note that PCM is normally designed to be written in a cache line size, e.g., 64 bytes, because processors usually include internal/on-chip (SRAM) cache and access byte-addressable off-chip DRAM or PCM in the unit of a cache line size as a batch; although byte updates to PCM are possible, they will be much less efficient than being updated in the cache line size.

Thus, in this work, the considered block sizes of file systems are multiples of the cache line size of PCM. In addition, the proposed strategy dynamically allocates space for inodes with the support of inode indirection to reclaim space of inodes efficiently, such that the space of inodes (or inode tables) and data blocks can be interchanged adaptively to resolve the external fragmentation caused by unused inodes or data blocks.

B. Phase Change Memory (PCM)

Phase change memory can be exploited by the memory system and by the convergence of consumer, computer and communication electronic systems. The caching of the existing reminiscence technologies, reducing the general device fee and device complexity could be the compelling motivation for PCM adoption. Bandwidth will power the sustaining side of PCM in code and data transfer packages and while reduction in strength dissipation will represent a further added cost of this technology. PCM is today's reminiscence leap forward. Like flash, PCM is a nonvolatile memory that could keep bits even without a strength supply.

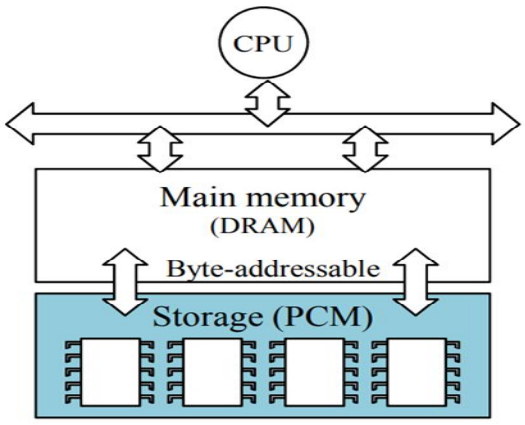


Fig1. Architecture for PCM based Storage system

But not like flash, statistics can be written to cells a great deal quicker, at charges corresponding to the dynamic and static random-get admission to reminiscence (DRAM and SRAM) used in all computer systems and mobile telephones these days. Quite virtually, PCM blends together the high-quality attributes of NOR flash, NAND flash, EEpROM and RAM handing over a new category of reminiscence for brand spanking new usage models.

C. Space Utilization

In a file system, we may have a number of small and large files as well as metadata that need to be stored. The space utilization efficiency is very important especially for SCM devices considering their expensive cost. We want to utilize superpages for storing data which may potentially reduce the pressure on TLB and improve file system performance. However, allocating the whole file system data with superpage will generate lots of internal fragmentation, especially for small files and metadata. In such a case, we may have low space utilization efficiency on the SCM device.

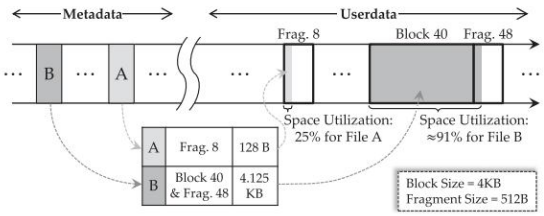
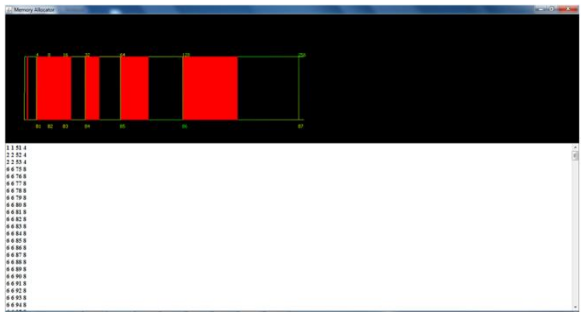


Fig2. Storage system for UNIX File System

The space utilization of inode-based file systems is strongly influenced by the number of used blocks and block sizes to store files. An inode based file system allocates data blocks for user data and indirect blocks for indirect pointers to maintain file contents. When a file size is large enough, inode-based file systems allocate indirect blocks to store the indirect pointers that (1) point to other indirect blocks or (2) point to the (data) blocks that store the content of the file. Hence, in inode-based file systems, the allocated storage space salloc for a file is dependent on the number of allocated/used data blocks and the number of allocated/used indirect blocks including single, double, and triple indirect blocks.

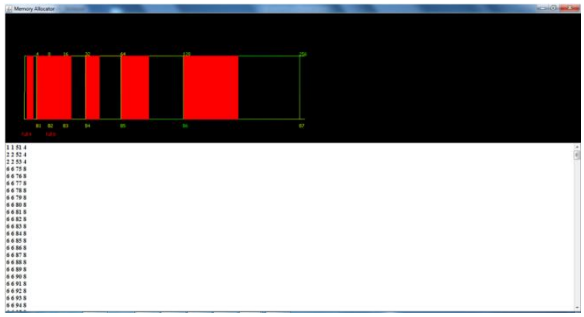
4. EXPERIMENTAL RESULTS

In this experiment, we upload a memory dataset and after uploading dataset we can run the normal fragmentation.



In normal fragmentation, it left the free block space. Hence, we can say normal fragmentation provide resource wastage.

In PCM fragmentation, it will verify the previous block if any free. By doing this, we can avoid the resource wastage problem.



5. CONCLUSION

In this paper we proposed multi-grained block management strategy to optimize the space utilization of file systems over PCM-based storage systems. By using this proposed strategy, we can reduce the space utilization in the file system. The proposed multi-grained block management strategy is allocating the proper block sizes in PCM to minimize the internal fragmentation issue.

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