SVPWM TECHNIQUE FOR FOUR-POLE INDUCTION-MOTOR DRIVE WITH SINGLE DC–LINK USING A QUAD TWO-LEVEL INVERTER

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Abstract: In this paper a new SVPWM technique is implemented along with multilevel inverter topology for a four-pole induction-motor drive; which is constructed using the induction-motor stator winding arrangement. In this process we are comparing with the conventional five-level inverter topologies so we are a single dc source with a less magnitude therefore, the power balancing problem are reduced. As this configuration uses a single dc source, and it also provides path for zero-sequence currents because of the zero-sequence voltages present at the output side, which will flow through the power electronic switches and motor phase winding. By using SVPWM Technique generates less harmonics distortion at output voltage and current and voltage utilization will more compare to other PWM technique. In this paper we are implementing SVPWM technique with the quad two level inverter topology is proposed and verified using the simulation results.

Index Terms—Induction-motor drive, space vector pulsewidth modulation (SVPWM), multilevel inverter, Overmodulation.

NOMENCLATURE
IVPWC Identical voltage profile winding coil.
SVPWMSine–triangle pulsewidth modulation.
Ias, Ibs, Ics Stator phase currents.
Rs Stator resistance.
Rr Rotor resistance.
Lls Stator leakage inductance.
Lss Stator self-inductance.
Llr Rotor leakage inductance.
Lrr Rotor self-inductance.
Lm Magnetizing inductance

R Reluctance.
L Mean length.
A Area of the core.
μ Permeability

1. INTRODUCTION

For the control of medium- and high-voltage[1] ac drive applications most widely used technology is multilevel inverter because it have better harmonic performance[2], less voltage stress on power electronic devices[3], and etc. The main reason to achieve the multilevel inverter is the staircase voltage waveform by using more low-rated power electronic switches and voltage sources. As the output voltage levels increase[4], then the requirement of series-connected switches will also increase in the case of conventional multilevel inverters such as diode-clamped and flying-capacitor (FC) multilevel inverters. More over if signal switch also fail any of the switches fails, then the entire topology will be fail then the resulting will be like this reduce the system reliability[5]. The topologies have the drawbacks like the neutral-point voltage balancing and capacitor voltage balancing problems, which may turn and cause unequal voltage sharing[6], across the switches and adds dc offset voltage to the output voltage waveform. To reduce this problem special capacitor voltage balancing techniques are needed. By using the H-bridge configuration[7], the reliability of the system can be increased. It may also reduce the neutral-point voltage balancing issue and capacitor voltage balancing issue, it requires more isolated dc sources when the number of voltage levels increase[8]. Another interesting topology the dual-inverter configuration using an open-end winding induction motor to increase the reliability of the system. In this configuration, the neutral point of the induction motor is disconnected, and both sides of the winding are fed from two-level (or multilevel) inverters

In this configuration, when compared with conventional neutral-point-clamped (NPC) or FC multilevel inverters we requires only half of the dc source voltage[9]. To reduce the aforementioned problems, such as capacitor voltage balancing and the requirement of more voltage sources, a five-level inverter topology are presented in this paper[10], which uses three dc sources for desired output wave form of a five-level voltage. In this paper, the designing the multilevel inverter topology[11] will use the advantage of two IVPWCs of a four pole induction motor. And the other side we use the open-end winding induction motor supplied by a SVPWM-controlled multilevel inverters with a single dc source which will provide path for the zero-sequence current because of its dominanton the lower order harmonic voltages in the inverter output voltage.

A five-level inverter topology for a four-pole Induction-motor drive with a single dc link is introduced in this paper along with combination of SVPWM technique[12] to reduce the generated harmonics distortion at the output voltage and current and voltage utilization will be more compare with other technique. Wide linear modulation range and

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Less switching loss. This paper, a modified SVPWM technique is proposed to operate the five-level inverter configuration (using quad two level inverters) also over modulation region. The proposed scheme is simulation verified, and results are then presented.

2. VOLTAGE EQUATIONS OF INDUCTION-MOTOR STATOR WINDING

We also known that, in this conventional ac machine, the winding of the coils which is about 360° (electrical) apart form the identical voltage profiles across them. Then, the four-pole induction motor consists of two IVPWCs (where the number of IVPWCs is equal to the number of pole pairs) and in the conventional four-pole induction motor and these two windings are connected in series, as shown in Fig. 1(a). moreover in this paper, there are disconnected, as shown in Fig. 1(b). As the two windings are disconnected exactly with an equal to the number of turns, which can be written [as shown in Fig. 1(a) and (b)] as

\[ N_1 = N_2 = \frac{N}{2} \]

Reluctance is given by [22]

\[ R = \frac{1}{\mu A} \]

From the following observations can be make the compared along with the conventional-induction-motor parameters.

a) Stator resistance \( r_s = p/\Omega \) will be half because of the length of the copper is half.

b) Reluctance offered to the leakage flux will be half because of the mean length of the stator leakage flux is half; from (1) and (2), we can say that the leakage inductance \( L_{1ls} = N_1 2/R \) will be half.

c) Reluctance offered to the magnetizing flux will be the same because of the mean length of the core will be same in both the cases. Therefore, from (1) and (2), the magnetizing inductance \( L_{ms} = N_1 2/R \) will be 1/4 times. From the above discussion and by writing KVL as shown in Fig. 1(b), the voltage across one IVPWC of A-phase can be obtained as

\[ V_{a1} - V_{a2} = \left( \frac{r_s}{2} \right) i_{as} + \left( \frac{L_{as}}{2} \right) p_{ias} - \left( \frac{1}{2} \right) \left( \frac{L_m}{2} \right) p_{i cs} \]

(3)

The voltage across the other IVPWC of A-phase can be obtained by writing the Kirchoff’s voltage law (KVL) shown in Fig. 1(b),

\[ V_{a3} - V_{a4} = \left( \frac{r_s}{2} \right) i_{as} + \left( \frac{L_{as}}{2} \right) p_{i as} - \left( \frac{1}{2} \right) \left( \frac{L_m}{2} \right) p_{i cs} \]

(4)

The effective voltage across the stator winding is the sum of the voltages across the two individual windings, i.e.

\[ V_as = (V_{a1} - V_{a2}) + (V_{a3} - V_{a4}) \]

(5)

The motor phase voltage can be achieved by substituting (3) and (4) into (5) as follows:

\[ V_{as} = r_s i_{as} + L_{as} p_{ias} - \left( \frac{1}{2} \right) L_m p_{i cs} \]

(6)

The voltage across the total winding of A-phase can be obtained by writing the KVL shown in Fig. 1(a), which is equal to the (6). It can be observed from the above discussion that (6) and the voltage equation of the conventional induction motor presented.

3. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The five-level inverter topology presented it uses the three dc sources to obtain the five-level voltage waveform. To providing dc supply diode bridge rectifiers are used here. Therefore, in regenerative braking, it requires three braking rheostats and three control mechanisms is used to protect the rectifier units, which complicate control and power circuits. In this paper, three dc sources are replaced by a single dc source, as shown in Fig. 2.
voltage blocking capacity of these switches is $V_{dc}/8$ only. All these (main and auxiliary) switches are switched in such a way to produce five-level voltage ($(V_{dc}/2), (V_{dc}/4), 0, (−V_{dc}/4), (−V_{dc}/2)$) across the motor phase winding, and the possible switching combinations are shown in Table I.

### Table I
Possible Switching Combinations To Generate Five-Level Voltage Waveforms

<table>
<thead>
<tr>
<th>Voltage Magnitude</th>
<th>$s_1$</th>
<th>$s_2$</th>
<th>$s_3$</th>
<th>$s_4$</th>
<th>$s_5$</th>
<th>$s_6$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$+V_{dc}/2$</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>$+V_{dc}/4$</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>0</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>$-V_{dc}/4$</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>$-V_{dc}/2$</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

The Permanent shorting of the bidirectional switches cause unequal voltages across IVPWCs during some ($(−V_{dc}/4),0,(V_{dc}/4)$) voltage-level synthesis. The control of these bidirectional switches is important, which is explained. The proposed multilevel inverter topology is compared along with the conventional five-level NPC inverter, FC inverter, and the cascaded H-bridge inverter, as shown in Table II.

### Table II
Comparison Between The Conventional Topologies With The Proposed Topology

<table>
<thead>
<tr>
<th></th>
<th>NPC</th>
<th>FC</th>
<th>H-bridge inverter</th>
<th>Proposed Topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main switches</td>
<td>24</td>
<td>24</td>
<td>24</td>
<td>24</td>
</tr>
<tr>
<td>Clamping Diodes</td>
<td>36</td>
<td>36</td>
<td>36</td>
<td>36</td>
</tr>
<tr>
<td>Isolated voltage sources</td>
<td>$V_{dc}$</td>
<td>$V_{dc}$</td>
<td>$V_{dc}$</td>
<td>$V_{dc}$</td>
</tr>
<tr>
<td>Capacitors tanks</td>
<td>4</td>
<td>18</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Bi-directional switches</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The magnitude of the dc bus requirement is also less ($V_{dc}/4$). The only additional requirement in this topology is six bidirectional switches with voltage rating of $V_{dc}/8$.

### IV. SPACE VECTOR PULSE WIDTH MODULATION

The main objectives of space vector pulse width modulation generated gate pulse are the following.
- Wide linear modulation range
- Less switching loss
- Less total harmonic distortion in the spectrum of switching waveform
- Easy implementation and less computational calculations

With the emerging technology in microprocessor the SVPWM has been playing a pivotal and viable role in power conversion (Jenni and Wueest 1993). It uses a space vector concept to calculate the duty cycle of the switch which is imperative implementation of digital control theory of PWM modulators. Before getting into the space vector theory it is necessary to know about the harmonic analysis of power converters. With the application of Fourier analysis the harmonic content of any waveform can be determined. A brief description of such analysis is presented here. This study is with a view to measure total harmonic distortion which will indicate the probable losses in the output.

#### A. Linear Modulation Region ($0 < m_i < 1$):

The Gating puls will be the proposed in the multilevel inverter are generated by using SVPWM with a real-time digital simulator. Along with the three modulating signals (sine waves) and the four carrier signals (triangular waves) are used and also to produce the gating pulses for the proposed topology, as shown in the Fig. 3.

![Fig. 3. Modulating and carrier waves for generating gating pulses in SPWM.](image)

The switching combinations shown in Table III give less switching transitions from one voltage level to another. And The remaining switching combinations (in Table I) are used in the case of fault condition, to increase the reliability of the system. In other the case of any switch failure of the middle two inverters (inverters 2 and 3), the entire system required not to be shut down.

### Table III
Comparison Of Carrier And Modulating Signals Corresponding To The Output Voltage

<table>
<thead>
<tr>
<th>Comparison between Modulating and Carrier signals</th>
<th>Output Voltage Level</th>
<th>Optimum switching combinations</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{m} &lt; V_{r1}$</td>
<td>$V_{dc}/2$</td>
<td>$V_{dc}$</td>
</tr>
<tr>
<td>$V_{r1} &lt; V_{m} &lt; V_{r2}$</td>
<td>$V_{dc}/4$</td>
<td>$V_{dc}/2$ and $V_{dc}/4$</td>
</tr>
<tr>
<td>$V_{r2} &lt; V_{m} &lt; V_{r3}$</td>
<td>$V_{dc}/8$</td>
<td>$V_{dc}/4$ and $V_{dc}/8$</td>
</tr>
<tr>
<td>$V_{r3} &lt; V_{m} &lt; V_{r4}$</td>
<td>$V_{dc}/16$</td>
<td>$V_{dc}/8$ and $V_{dc}/16$</td>
</tr>
<tr>
<td>$V_{m} &gt; V_{r4}$</td>
<td>$V_{dc}/32$</td>
<td>$V_{dc}/16$ and $V_{dc}/32$</td>
</tr>
</tbody>
</table>

Instead, it can be operated as a three-level inverter up to a modulation index will be 0.5 (where modulation index is equal to the ratio of the peak of the modulating signal to four times the peak of the carrier signal, as shown in Fig. 3). We can see For
example, when switch S21 is open (or S22 is shorted), the possible switching combinations as shown in Table IV

Table IV
Possible Switching Combinations During Fault Condition

<table>
<thead>
<tr>
<th>Voltage Magnitude</th>
<th>S_{11}</th>
<th>S_{21}</th>
<th>S_{12}</th>
<th>S_{22}</th>
<th>S_{1}</th>
<th>S_{2}</th>
</tr>
</thead>
<tbody>
<tr>
<td>$+\frac{V_{dc}}{4}$</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>0</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>$-\frac{V_{dc}}{4}$</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

B. Over modulation ($m_i > 1$):

The linear modulation region can be significantly increased by adding the zero-sequence component to the modulating signals in SVPWM. Due to the addition of the zero sequence component, then the sum of instantaneous reference phase signals will be not equal to the zero ($V_a + V_b + V_c = 0$), which can also used to produce lower order zero-sequence currents in the motor phase windings. Therefore, the SVPWM technique is best suitable for those configurations which can able to provide a closed path for the zero sequence currents (generally, open-end winding induction motor drives with a single dc link). The subtracted magnitude of the A-phase signal (i.e., $V_a - V_{tp}$ as shown in Fig. 4) is proportionally added to the B-phase and C-phase modulating signals such that the sum of the three phase modulating signals will be equal to zero ($V_a + V_b + V_c = 0$). Then the same procedure will followed along with the B-phase and the C-phase. As well as we known that when the modulation index may be varying between 1 to $2/\sqrt{3}$, and the maximum of one phase modulating signal crosses the peak of the upper carrier signal, and for a modulation index greater than $2/\sqrt{3}$, the maximum of two or three phase modulating signals cross the peak of the carrier signal simultaneously. Therefore, by using the proposed method, it may be possible to operate the drive in the over modulation region up to the modulation index of $2/\sqrt{3}$. Beyond this modulation index, as two modulating signals are crossing the peak of the carrier wave simultaneously, which may results the considerable reduction in the fundamental component. The line-to-line modulating signals are as shown in Fig. 5 for different modulation indexes we demonstrate the maximum possible limit of the modulation index. And It is clearly from shown in Fig. 5(a) and (b) that the fundamental voltage magnitude will be increasing from the modulation index about the 1 to $2/\sqrt{3}$ and it may starts decreasing from $2/\sqrt{3}$, as shown in Fig. 5(c) and (d).

Fig. 5. Three phase line-to-line modulating waves in over modulation after compensation. (a) $m_i = 1$, (b) $m_i = 1.15$, (c) $m_i = 1.25$, and (d) $m_i = 1.5$.

In the proposed method, the average value of the line-to line modulating signal will be calculated by the assuming $V_{tp} = 1$. And then The expression for the line-to-line modulating signal will be written from the Fig. 4 (dotted lines) and the integrated from $\pi/3$ to $5\pi/6$ (since the waveform is followed by the quarter-wave symmetry, and from any $90^\circ$ will be the duration which can be considered) to get the average value; which is given in (7), shown at the bottom of the page, where

$$X_1 = V_m \sin \left( \omega t - \frac{2\pi}{3} \right) + V_m \sin \left( \omega t + \frac{2\pi}{3} \right)$$  \hspace{1cm} (7)

$$X_2 = V_m \sin (\omega t) + V_m \sin \left( \omega t - \frac{2\pi}{3} \right)$$  \hspace{1cm} (8)

The expression for the line-to-line modulating signal in conventional SPWM over modulation is also written from Fig. 4 (solid lines) and integrated from $\pi/3$ to $5\pi/6$.

Fig. 6. Percentage magnitude reduction of the line-to-line modulating signal with respect to the modulation index.
Where The percentage reduction in the line-to-line modulating signal is calculated, and it is plotted for different modulation indexes, as shown in Fig. 6. It can be noticed in Fig. 6 that the loss in line-to-line voltage is at the maximum of 2%, which is negligible.

V. SIMULATION RESULT

The proposed multilevel inverter is verified by using the simulation results with a 5-hp four-pole induction motor. The gating pulses to the proposed multilevel inverter are generated using SVPWM technique.

Fig. 7(a) shows the simulation results for the modulation index of 0.4. The voltage across the motor phase winding is the sum of the voltage across the individual windings.

Fig. 8. Top trace is the inverter-1 pole voltage, the second trace is the inverter-4 pole voltage, the third trace is the voltage between the middle two inverters, and the bottom trace is the voltage across bidirectional switch for the modulation index of (a) 0.4 [y-axis 100 V/div; x-axis 25 s/div] and (b) 0.8 [y-axis 100 V/div; x-axis 5 ms/div].

As shown in fig 9(a), which demonstrate the validity of the proposed configuration in the over modulation region using the modified SPWM technique. The zero sequence currents flowing through motor phase windings are close to zero.

Results for the same modulation index with a conventional SPWM technique are presented. Fig. 9(a) and (b) that zero-sequence currents are significantly low in the proposed PWM technique. In the case of any switch failure of inverter 2 or 3, the proposed topology need not be shut down; instead, it can be operated as a three-level inverter up to the modulation index of 0.5, as shown in Fig. 10, thereby increasing the reliability of the system when compared with conventional five-level (NPC or FC) inverters.
Fig. 9. Top trace is the voltage across the first winding (Va1–Va2), the second trace is the voltage across the second winding (Va3–Va4), the third trace is the effective voltage across the total stator phase winding, and the bottom trace is the stator current (Ia) for the modulation index of 0.5 during fault condition [y-axis 100 V/div, 2 A/div, x-axis 10 ms/div].

(a)

(b)

Fig. 10. Top trace is the voltage across the first winding (Va1–Va2), the second trace is the voltage across the second winding (Va3–Va4), the third trace is the effective voltage across the total stator phase winding, and the bottom trace is the stator current (Ia) for the modulation index of 0.5 during fault condition [y-axis 100 V/div, 2 A/div, x-axis 5 ms/div].

(a)

(b)

CONCLUSION
A multilevel inverter topology has been presented for a four-pole induction-motor drive is implemented in this paper. All these four two-level inverters are connected along the single dc source decreasing the power balancing issues. The magnitude of dc source voltage requirement will be very less when compared along with the conventional five-level inverter topologies. This topology will only use the two-level inverters; therefore, it has the freedom from capacitor voltage balancing issues. And the proposed topology is verified with a 5-hp four-pole induction motor by using simulation results.

The Gating pulses are generated using the SVPWM technique for the linear modulation region and for the overmodulation region and by using the modified SVPWM technique. During the case of any switch failure of the middle two inverters, the topology will be operated by the three-level inverter up to the modulation index of 0.5. This will increase the reliability of the system during fault condition when compared with conventional NPC or FC topologies. This concept can also be applied to obtain a higher number of voltage levels for the induction motor along with the higher number of poles, it may require more two-level inverters.

REFERENCES


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