A NEW TECHNIQUE OF HFL FOR BIDIRECTIONAL BUCK–BOOST DC–DC CHOPPER-MODE INVERTERS USING FUZZY LOGIC CONTROLLER

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Abstract - A circuit configuration and the circuit topological family of HFL for bidirectional buck–boost dc–dc chopper-mode inverters using Fuzzy logic controller is proposed in this paper. The steady principle characteristic and therefore the criterion for the key circuit parameters with fuzzy logic got during this paper. The circuit configuration consists of 2 identical isolated duplex buck-boost dc–dc choppers with an equivalent input and output filters. These 2 choppers in parallel at input finish and serial at output finish generate unipolarity curved pulse breadth modulation current waveforms with positive and negative [*fr1] low frequency cycles on an individual basis. The circuit topological family includes four circuit topologies, like one-transistor mode. A circuit configuration, a circuit topological family, a buck-mode active clamped circuit, and an on the spot output voltage feedback management strategy of combined duplex buck-boost dc–dc chopper-mode electrical converter with high-frequency (HF) link (HFL) were projected and absolutely investigated during this paper. Taking the one-transistor mode circuit topology as Associate in Nursing example, the 750VA48VDC/220V50HzAC example is meant and enforced. The theoretical analysis and principle take a look at how the inverters have glorious performance.

Index Terms—Bidirectional power flow, buck–boost dc–dc chopper, Fuzzy logic controller, buck-mode active clamped circuit, high-frequency (HF) link, inverter, single-stage power conversion.

I INTRODUCTION

The bidirectional buck–boost dc–dc converter has important value on theory and application in power conversion fields with bidirectional power flow, such as electrical vehicles, photo voltaic power supply systems of satellites, battery charging and discharging, standby power supplies, etc. The buck–boost dc–dc converter has advantages such as simple topology, higher reliability under overload or short-circuit conditions, and wide use in the low power field [1]–[3]. However, this converter has an inherent defect, i.e., the leakage inductance energy of the high-frequency (HF) storage transformer needs to be absorbed and inhibited. An isolated buck–boost dc–dc converter with excellent performance was obtained through active clamped or resonant technology. In particular, there are more problems to be solved in the isolated bidirectional dc–dc converter [8]. A unidirectional buck–boost mode inverter with HF link (HFL) has the features of simple topology, discontinuous operating mode, large total harmonic distortion of the output current, low conversion efficiency, and low output power [9]. A differential buck–boost dc–dc converter mode inverter with HFL has the features of two-stage conversion, circulating current between two converters, and low efficiency [10]. A novel circuit configuration and the circuit topological family of the combined bidirectional dc–dc chopper mode inverters with HFL are proposed in this paper. The inverter with HFL, which has only single-stage power conversion and high conversion efficiency, can be widely used in the inverting fields such as those with dc generators, batteries, photovoltaic cells, etc.

II CIRCUIT TOPOLOGY FAMILY AND CONTROL STRATEGY

A. CIRCUIT CONFIGURATION AND CIRCUIT-TOPOLOGY FAMILY

A circuit configuration and the circuit topological family of combined bidirectional buck–boost dc–dc chopper-mode inverters with HFL were proposed in this paper, as shown in Fig. 1. While chopper I outputs unipolarity sinusoidal pulselwidth modulation (SPWM) current waveforms io1 with positive half low-frequency (LF) cycle, chopper II is shut down and freewheeling switch S25 is conducted, io2 = 0, and chopper I generates the positive half cycle of sinusoidal voltage uo filtered by capacitor Cf. Conversely, while chopper II outputs unipolarity SPWM current waveforms io2 with negative half LF cycle, chopper I is shut down and freewheeling switch S15 is conducted, io1 = 0, and chopper II generates the half cycle of uo filtered by Cf. The inverter has single-stage power conversion since only
one chopper is working at any time. When the power flow is from source to the load, i.e., \( i_{o1} > 0 \) or \( i_{o2} > 0 \), the input dc voltage \( U_i \) is inverted to unipolarity HF ac pulse currents \( i_{i1} \) and \( i_{i2} \) by the inverter. After the galvanic isolation, transmission, and current match by the HF storage transformers \( T_1 \) and \( T_2 \), \( i_{i1} \) and \( i_{i2} \) are rectified into unipolarity HF ac pulse currents \( i_{o1} \) and \( i_{o2} \) by the rectifier. Then, \( i_{o1} \) and \( i_{o2} \) are filtered into high-quality LF sinusoidal voltage \( u_o \) in ac load \( Z_L \) by capacitor \( C_f \). \( i_{i1} \) and \( i_{i2} \) are filtered into smooth dc input current \( i_i \) by the input filter. When the power flow is from the load to source, i.e., \( i_{o1} < 0 \) or \( i_{o2} < 0 \), the rectifying switches are operating at inversion and the inverting switches are operating at rectification. A circuit topological family of the proposed inverter includes four circuit topologies, namely, one-transistor mode, two-transistor mode, interleaved one-transistor mode, and interleaved two-transistor mode, as shown in Fig. 1(b)–(e). The voltage stress of the power switches in the input inverter side of

![Circuit Configuration and Circuit Topological Family of the Combined Bidirectional Buck-Boost DC-DC Chopper-Mode Inverter with HFL. (a) Circuit Configuration. (b) One-Transistor Mode. (c) Two-Transistor Mode. (d) Interleaved One-Transistor Mode. (e) Interleaved Two-Transistor Mode.](image)
corresponding logical and delay conversions of \( u_{k1}, u_{k2}, u_{s}, u_{us}, u_{sy}, \) and \( u_{sy} \). The output voltage can be adjusted and kept stable by adjusting the modulation depth of the dc chopper and the amplitude of error signal \( u_e \) when the input voltage \( U_i \) or load \( Z_L \) varies.

III STEADY PRINCIPLES AND OUTPUT CHARACTERISTIC

A. FOUR OPERATION MODES IN ONE LF CYCLE

According to the direction of the chopper’s power flow, the proposed inverter has four operation modes A, B, C, and D in one LF cycle, as shown in Table I. When analyzing operation modes, the inverter’s load is the equivalent load of \( C_f \) and \( Z_L \) in parallel. Due to space constraints, this paper will analyze a one-transistor mode shown in Fig. 1(b) under equivalent inductive load. The steady principle waveform of the proposed inverter in one LF output voltage period is shown in Fig. 3. Under equivalent inductive load, both load current \( i_o \) and the fundamental component of equivalent load current \( i_{oe1} \) lag behind output voltage \( u_o \).

![Fig. 2. Steady principle waveforms of the inverter in low-frequency cycle.](image)

1) \( t = [t_0−t_1] \): \( u_o > 0, i_{oe1} < 0 \), chopper I is working and chopper II is shut down, and the inverter is operating in mode B. \( S_{13} \) is HF chopping, \( S_{11} \) is HF conducted complementarily, and \( S_{25} \) is conducted. Equivalent load feeds energy back to the source by chopper I.

2) \( t = [t_1−t_2] \): \( u_o > 0, i_{oe1} > 0 \), chopper I is working, chopper II is shut down, and the inverter is operating in mode A. \( S_{11} \) is HF chopping, \( S_{13} \) is HF conducted complementarily, and \( S_{25} \) is conducted. The source outputs energy to the equivalent load by chopper I.

3) \( t = [t_2−t_3] \): \( u_o < 0, i_{oe1} > 0 \), chopper I is shut down and chopper II is working, and the inverter is operating in mode D. \( S_{23} \) is HF chopping, \( S_{21} \) is HF conducted complementarily, and \( S_{15} \) is conducted. Equivalent load feeds energy back to the source by chopper II.

4) \( t = [t_3−t_4] \): \( u_o < 0, i_{oe1} < 0 \), chopper I is shut down, chopper II is working, and the inverter is operating in mode C. \( S_{21} \) is HF chopping, \( S_{23} \) is HF conducted complementarily, and \( S_{15} \) is conducted. The source outputs energy to the equivalent load by chopper II.

The operation modes’ sequence of the proposed inverter under equivalent inductive load is B-A-D-C. Similarly, the resistive and capacitive loads are A-C and A-B-C-D, respectively. A special case is the resistive load, whose intervals of energy feedback operation modes B and D are short.

<table>
<thead>
<tr>
<th>Operation Modes</th>
<th>Chopper I</th>
<th>Chopper I</th>
<th>Power Flow Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Operating</td>
<td>Shut-down</td>
<td>Positive</td>
</tr>
<tr>
<td>B</td>
<td>Operating</td>
<td>Shut-down</td>
<td>negative</td>
</tr>
<tr>
<td>C</td>
<td>Shut-down</td>
<td>Operating</td>
<td>Positive</td>
</tr>
<tr>
<td>D</td>
<td>Shut-down</td>
<td>Operating</td>
<td>negative</td>
</tr>
</tbody>
</table>

B. SWITCHING STATE EQUATIONS

The equivalent circuits of the proposed inverter in the positive or negative half cycle of the output voltage are bidirectional buck–boost dc–dc chopper I and chopper II separately. Taking one-transistor mode circuit in Fig. 1(b) as an example, suppose that \( r_1 \) is the equivalent resistance including the primary winding resistance of the HF storage transformer and the on resistance of \( S_{11} \) (\( S_{21} \)); \( r_2 \) is the equivalent resistance including the secondary winding resistance of the HF storage transformer and the on-resistance of \( S_{13} \) (\( S_{23} \)) and \( S_{25} \) (\( S_{15} \)); and \( d \) is the duty cycle.
By multiplying (1) by d and then adding the result of multiplying (2) by \((1 - d)\), assuming \((dii/dt) = 0, (d00/dt) = 0, (di0/dt) = 0\), \(L1/L2 = (N1/N2) \), \(N111 = N2101\), \(r1/r2 = (N1/N2) \), and \(RL = U0/I0\), the steady-state values of the state variables are given by

\[
U_0 = \frac{N2}{N1} \frac{U_1}{1 - D} \frac{I_{g2}}{(1 - D)^2} \\
I_{11} = \left(\frac{N2}{N1}\right)^2 \frac{U_1 D}{(1 - D)^2 R_L + r_2} \\
I_{21} = \left(\frac{N2}{N1}\right)^2 \frac{U_1 D}{(1 - D)^2 R_L + r_2}
\]

Similarly, the current is derived by

\[
I_{12} = \left(\frac{N2}{N1}\right)^2 \frac{U_1 D}{(1 - D)^2 R_L + r_2}
\]

C. STEADY OUTPUT CHARACTERISTICS

Because \(S11\) (\(S21\)) and \(S13\) (\(S23\)) are HF conducted complementarily, there is only continuous current mode (CCM). The primary inductance current has three kinds of situations: the initial value is greater than zero; the initial value is less than zero and the final value is greater than zero; and the initial and final values are both less than zero. Since the inductance current only has CCM, the ideal steady \((r1 = r2 = 0\) output characteristic of the inverters is given by

\[
U_0 = \frac{N2}{N1} \frac{D}{1 - D} U_1
\]

When the initial value of the primary inductance current is zero, the load current is

\[
I_0 = I_{d0} = \frac{N2}{N1} \frac{D}{1 - D} \frac{U_1}{2 L_1}
\]

IG is maximal when \(D = 1/2\) from the aforesaid equation. The maximum of IG is

\[
I_{G\text{max}} = \frac{N2}{N1} \frac{D}{1 - D} \frac{U_1}{2 L_1}
\]

From (6) and (8), when the initial value of the primary inductance current is equal to zero, the ideal output characteristic of the proposed inverter is derived

\[
U_0 = \frac{N2}{N1} \frac{D}{1 - D} U_1
\]
\[ I_C = 4I_{G \text{ max}}D(1 - D) \]  

(9)

The rated output characteristics \( u_o/(U_iN_2/N_1) = f(i_o/I_{G \text{ max}}) \) of the proposed inverter is shown in Fig. 4. When \( u_o > 0 \) the output characteristic curve is in the upper half-plane of Fig 4 D is the duty cycle of chopper.}

IV RESTRAINT OF TURN-OFF VOLTAGE PEAKS OF POWER S WITCHES

A. BUCK-MODE ACTIVE CLAMPED CIRCUIT

A new buck-mode active clamped circuit is proposed to restrain the turn-off voltage peaks of S11 and S21, as shown in Fig. 5, which is composed of Dc1, Dc2, and Dc, clamped capacitance Cc, clamped switch Sc, filtering inductance Lc, and Ci. Two snubber circuits consisting of R13 and C13, R23 and C23, respectively, restrain the turn-off voltage peaks of S13 and S23. When the inverter is transmitting power flow at the positive and negative directions, voltage peaks caused by leakage inductance exist in S11 (S12) after being turned off in every switching cycle, which can make Dc1 (Dc2) conductive. In addition, the leakage inductance energy of T1 charges Cc. When the terminal voltage of Cc increases to a set value, Sc is conducted and the energy feeds back to the source. Udsc increases to Cc’s voltage value then stays constant. \( t=t_1-t_2: S11 \) is turned off at t1. S11’s junction capacitor is charging. The terminal voltage Ud1 and ii1 increase. \( t=t_2-t_3: uds11 \) increases to Cc’s voltage value then stays constant. \( t=t_3-t_4: uds13 \) decreases to zero at t3. ii1 decreases to zero. Io1 flows through S13’s body diode and starts to decrease positively. The stored energy of T1 releases to the load via S13’s body diode. \( t = t_4-t_5: S13 \) is turned on at t4. When S13’s voltage drop is smaller than that of the body diode, S13 realizes ZVS.

B. ANALYSIS OF HF SWITCHES’ OPERATING PROCESS

The primary winding voltage u11 is negative. ii1 decreases positively, and io1 increases from zero. The voltage peak of uds11 caused by the resonance between the leakage inductance and S11’s junction capacitance is bigger than UoN1/N2 + Ui, which makes Dc1 positively turned on. The leakage energy is passed to Cc via Dc1. Udsc and udsc increase until Dc1 is reversely turned off. Taking chopper I as an example, under an entirely positive power flow, when iLc is continuous, the principle waveforms of one Ts includes ten intervals, as shown in Fig. 6

\[ \frac{N_2}{N_1} = \frac{V_{U \text{ rms}}(1 - D_{\text{max}})}{D_{\text{max}}U_{i_{\min}}} \]  

(10)

V DESIGN CRITERIA OF THE KEY CIRCUIT PARAMETERS

A. HF STORAGE TRANSFORMER TURN RATIO

When input voltage Ui = Umin, D = Dmax and the peak output voltage \( u_o = \sqrt{2}U_{\text{rms}} \), determined by (6). The turns ratio of the HF storage transformer is given by
B. CURRENT STRESS OF POWER SWITCHES

From (6), the variation law of duty cycle $d$ is derived by

$$
d(t) = \frac{\sqrt{2}U_{\text{rms}} s \sin t}{U_j N_2/N_1 + \sqrt{2}U_{\text{rms}} s \sin t} \quad (11)
$$

The current flowing through S11 (S12) is the primary inductance current of the HF storage transformer. The peak, instantaneous, and effect values, respectively, are

$$
I_{t1\max}(n) = \frac{P_o(n)}{\eta U_j D(n)} + \frac{U_j L_1}{L_2} [t - (n - 1)T_s]
$$

$$
i_{t1}(t) = i_{t1\max}(n) - \frac{D(n)U_j}{L_2} + \frac{U_j}{L_2} [t - (n - 1)T_s + D(n)T_s]
$$

$$
(n - 1)T_s \leq t \leq (n - 1)T_s + D(n)T_s
$$

$$
i_{t1\text{rms}}(n) = \sqrt{\frac{1}{T_s} \int_{(n-1)T_s}^{(n-1)T_s+D(n)T_s} i_{t1}(t)^2 dt} \quad (13)
$$

In (12), $\eta$ is the conversion efficiency of the nth switching period. The effect value of $i_{t1}$ in one LF cycle is

$$
i_{t1\max} = \sqrt{\frac{1}{T_s} \sum_{n=1}^{N/2} i_{t1\text{rms}}(n)^2 T_s} \quad (15)
$$

where $N = T_o/T_s$ is the number of the HF switching periods in one LF cycle $T_o$. The current of S13 (S25) is the secondary inductance current of the HF storage transformer, the same with the current of switch S23 (S15). The peak, instantaneous, and effect values in the nth Ts are, respectively, given by

$$
I_{o1\max}(n) = \frac{N_1}{N_2} I_{t1\max}(n) \quad (16)
$$

$$
i_{o1}(t) = I_{o1\max}(n) - \frac{U_o(n)}{L_2} [t - (n - 1)T_o - D(n)T_o]
$$

$$
(n - 1)T_o + D(n)T_o < t < nT_o
$$

$$
i_{o1\text{rms}}(n) = \sqrt{\frac{1}{T_o} \int_{(n-1)T_o+D(n)T_o}^{nT_o} i_{o1}(t)^2 dt} \quad (18)
$$

The effect value of $i_{o1}$ in one LF cycle is calculated [refer to (15)].

C. DESIGN OF BUCK-MODE ACTIVE CLAMPED CIRCUIT

Every switching period, the stored energy of the primary leakage inductance $I_{\text{leak}}$ of the HF transformer is absorbed by

![Diagram of control circuit of active clamped switch](image)

Fig. 7. Control circuit of active clamped switch SC.

The junction capacitor $C_s$ of S11 (S21) and $C_c$, namely

$$
\frac{1}{2} (C_s + C_c) I_{Cs}^2 f_s = \frac{1}{2} C_c I_{Cc}^2 f_s
$$

$$
= \frac{1}{2} I_{t1\text{rms}}^2 + f_s \quad (19)
$$

In (19), $U_{Cc1}$ and $U_{Cc2}$ are, respectively, the before and after-charging voltages of $C_c$ in every Ts. The maximum drain–source voltage of S11 (S21) can be limited to $\sqrt{2}U_{\text{rms}} N_1/N_2 + U_i \max$ when $C_c$ is large enough. Thus, $C_c$ is given by

$$
C_c = \frac{L_{t1\max} I_{t1\text{rms}}^2}{\sqrt{2}U_{\text{rms}} N_1/N_2 + U_i \max} \quad (20)
$$

D. VOLTAGE AND CURRENT STRESSES OF ACTIVE CLAMPED SWITCH

The voltage stress of the switch SC is given by

$$
u_{sc} \geq \frac{N_1}{N_2} \sqrt{2}U_{\text{rms}} + U_i \max \quad (21)
$$

The current stress of SC can be approximately calculated by the feedback energy and clamped capacitor voltage.

E. CONTROL OF ACTIVE CLAMPED SWITCH SC

The control circuit of the clamped switch SC is shown in Fig. 7. The constant-frequency clock signal with fixed duty cycle is generated by comparing the triangle carrier signal $u_c$ with the dc reference voltage $u_b$. When the sampling signal $k u_{Cc}$ ($k$ is the voltage-dividing coefficient) of the clamped capacitor voltage is higher than the set value $u_b$, the control signal $u_{gsc}$ of SC can be obtained; if not, SC will shut down. $u_b$ should be set according to the maximum of $U_i$ and $u_o$ and is given by

$$
u_b = \left(\sqrt{2}U_{\text{rms}} N_1/N_2 + U_i \max\right) \times \frac{1}{50} \quad (22)
$$

FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC. The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication
using Mamdani’s, ‘min’ operator. v. Defuzzification using the height method.

**Fuzzification:** Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The partition of fuzzy subsets and the shape of membership CE(k) E(k) function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor.

In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular E(k) input there is only one dominant fuzzy subset. The input error for the FLC is given as

\[ E(k) = \frac{P_{\phi(k)}}{V_{\phi(k)}} - \frac{P_{\phi(k-1)}}{V_{\phi(k-1)}} \]  

(23)

\[ CE(k) = E(k) - E(k-1) \]  

(24)

**Table II Fuzzy Rules**

<table>
<thead>
<tr>
<th>CE</th>
<th>E</th>
<th>NB</th>
<th>NS</th>
<th>ZE</th>
<th>PS</th>
<th>PB</th>
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<td>PS</td>
<td>PB</td>
<td>PB</td>
<td>PB</td>
<td>PB</td>
</tr>
</tbody>
</table>

**Inference Method:** Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

**Defuzzification:** As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height” method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained.
SIMULATION RESULTS

The designed prototype: input voltage $U_i = 40\text{–}60$ V, output voltage $U_o = 220$ V/50 Hz, rated capacity $S = 750$ VA, switching frequency $f_s = 50$ kHz, maximum duty cycle $D_{\text{max}} = 0.65$, soft ferrites core LP3 PM 62 $\times$ 49 for T1, T2 (N2/N1 = 34/8), air gap of 3.8 mm, input filtering capacitor $C_i = 6 \times 2200$ $\mu$F, output filtering capacitor $C_f = 9.4$ $\mu$F, clamped capacitor $C_c = 0.47$ $\mu$F, clamped inductor

<table>
<thead>
<tr>
<th>Type</th>
<th>Conversion Ratio</th>
<th>Input Voltage</th>
<th>Output Voltage</th>
<th>Rated Output Power</th>
<th>Output Voltage THD</th>
<th>Efficiency of Rated Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-bridge inverter</td>
<td>$V_i / V_o$, $I_i / I_o$</td>
<td>21 V</td>
<td>103 V</td>
<td>100 W</td>
<td>3%</td>
<td>95%</td>
</tr>
<tr>
<td>Half-bridge inverter</td>
<td>$V_i / V_o$, $I_i / I_o$</td>
<td>120 V</td>
<td>120 V</td>
<td>150 W</td>
<td>2.3%</td>
<td>98%</td>
</tr>
<tr>
<td>HFL input–dc link inverter</td>
<td>$V_i / V_o$, $I_i / I_o$</td>
<td>320 V</td>
<td>120 V</td>
<td>300 W</td>
<td>3.1%</td>
<td>86%</td>
</tr>
<tr>
<td>AC–AC connection with HFL</td>
<td>$V_i / V_o$, $I_i / I_o$</td>
<td>220 V</td>
<td>120 V</td>
<td>300 W</td>
<td>2.1%</td>
<td>86%</td>
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<tr>
<td>The proposed push–pull inverter</td>
<td>$V_i / V_o$, $I_i / I_o$</td>
<td>48 V</td>
<td>220 V</td>
<td>180 W</td>
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<td>93.3%</td>
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<tr>
<td>The proposed full-bridge inverter</td>
<td>$V_i / V_o$, $I_i / I_o$</td>
<td>220 V</td>
<td>120 V</td>
<td>300 W</td>
<td>2.1%</td>
<td>86%</td>
</tr>
</tbody>
</table>

CONCLUSION

A circuit configuration and the circuit topological family of HFL for bidirectional buck–boost dc–dc chopper-mode inverters using Fuzzy logic controller is proposed in this paper. The circuit topological family includes four circuit topologies and adopts the instantaneous output voltage feedback control strategy and in the LF cycle the inverter has four operation modes. At the input end the circuit configuration of the inverter is composed of two identical isolated bidirectional buck–boost dc–dc choppers is proposed in this paper. At the output end which generate unipolarity SPWM current with positive and negative half LF cycles separately are connected in series. The steady principle
characteristic curve and the circuit parameters of the inverter are obtained. The turn-off voltage peaks are inhibited by the active clamped circuit. By using the simulation results we can analyze the inverters have advantages of HF galvanic isolation, simple topology, single-stage power conversion, high efficiency, strong adaptability to various loads, etc and also improve the conversion efficiency with fuzzy logic controller.

REFERENCES


