A NEW MODULATION STRATEGY AND VOLTAGE BALANCING CONTROL FOR MODULAR MULTILEVEL CONVERTERS WITH IMPROVED CONTROL SYSTEM

Fahad Bin Nahadi  
PG Scholar  
AL Habeeb College of Engineering and Technology, Hyderabad, India.  
fahad.nahdi1991@gmail.com,

Sri. V Chandra Shekhar  
Assistant professor  
AL Habeeb College of Engineering and Technology, Hyderabad, India,  
chandrashekar.vadla207@gmail.com

Sri.Karimulla Peerla Shaik  
Associate Professor  
AL-Habeeb College of Engineering and Technology, Hyderabad, India.  
karim.02214@gmail.com

ABSTRACT-The modular multilevel converter (MMC) has drawn attention due to its advantages of modular design, high efficiency and scalability, and excellent output waveforms with low harmonic distortion. For future high-power applications Modular multilevel converter(MMC) has become one of the most promising converter topologies. One of the special characteristics of the MMC is the common-mode current which usually includes a dc component and even-order (mainly the second-order) harmonic component and also good overall control system is also vital for the MMC. A challenging issue of the MMC is the voltage balancing among arm capacitors. A new method for voltage balancing among arm capacitors, which is based on an improved pulse-width modulation, is also presented . It avoids some major disadvantages found in present voltage balancing methods, such as dependence on computation-intensive voltage sorting algorithms, extra switching actions, interference with output voltage, etc. For both voltage-based and energy-based control methods a control structure for MMC inverters is presented in this paper, which is suitable, and includes voltage balancing between the upper and lower arms. By using the simulation results verify the effectiveness of the proposed methods.

INTRODUCTION

A new method for voltage balancing among arm capacitors, which is based on an improved pulse-width modulation, is also presented in this paper. Recently, multilevel converters have attracted growing attentions and found themselves of high power and high/medium voltage applications such as high-voltage dc transmission (HVDC), flexible ac transmission systems (FACTS), industrial motor drives, utility-scale renewable energy systems, and so on. Among various multilevel converters, the diode-clamped or neutral-point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) are the most studied topologies. Due to its modular structure the CHB topology then seems more suitable. However, for the applications requiring more than four or five levels, the NPC and FC topologies become less attractive due to significantly increased number of clamping diodes or FCs, higher power losses, and difficulty to balance the capacitor voltages.

A new centralized capacitor voltage balancing method along with an improved modulation method is proposed in this paper. This method as a whole has the following features:

1) In each arm of the MMC, compared with CPSPWM and conventional PDPWM only one voltage reference and one carrier are needed, which greatly reduces hardware requirement.

2) Among the power devices The SMs in one arm switch ON and OFF alternately, yielding an even distribution of switching frequency, and, therefore, a good inherent voltage balancing capability.

3) In a closed-loop manner accurate voltage balancing is achieved.

4) In this paper unnecessary switching actions and high-frequency voltage sorting problem are both avoided. Modeling and control of the overall MMC system are also investigated.
under all operating conditions. Deng et al. proposed another centralized method with CPSPWM. It does not need to measure the arm currents, therefore the cost is reduced. However, high-frequency voltage sorting still remains. Moreover, when the number of SMs is large, this method is heavily dependent on high switching frequencies, which may not be possible.

**MODELING AND CONTROL STRUCTURE**

**A. Converter Topology**

Fig. 1 shows the topology of a typical three-phase MMC. Each phase leg of the MMC consists of two arms. Each arm has N identical SMs and one smoothing inductor. Each SM has two power semiconductor switches (S1 and S2) representing two IGBTs (or other types) with freewheeling diodes and one capacitor (C).

**B. Modeling and Control Structure**

The SMs in each arm can be regarded as controlled voltage sources, and they are connected in series to form a controlled voltage source with higher voltage $v_P X$ and $v_N X (x = u - w)$. $i_P X$ and $i_N X$ are currents of the upper and lower arms. $V_{dc}$ and $I_{dc}$ are dc-link voltage and current. $v_{xis}$ ac-output voltage of phase $x$ (with respect to the midpoint of the dc-link). 

**1) Voltage /Current Control at AC Side:**

According to Kirchhoff’s voltage law

$$\begin{align*}
\frac{1}{2} V_{dc} &= v_{P X} + L \frac{\text{d} i_{P X}}{\text{d} t} + R i_{P X} + v_x \\
\frac{1}{2} V_{dc} &= v_{P X} + L \frac{\text{d} i_{P X}}{\text{d} t} + R i_{P X} - v_x
\end{align*}$$

(1)

According to Kirchhoff’s current law (KCL), ac current $i_x$ can be expressed as

$$i_x = i_{P X} - i_{N X}$$

(2)

Define a control variable $v_{1X}$ as

$$v_{1X} = \frac{1}{2} (v_{P X} - v_{N X})$$

(3)

Substituting (2) and (3) into (1) yields

$$\frac{1}{2} L \frac{\text{d} i_{P X}}{\text{d} t} + \frac{1}{2} R i_{P X} = -v_x - v_{1X}$$

(4)

In a closed-loop for grid-connected applications, the ac current ($i_x$) is usually controlled. With this structure, all the current control methods in conventional two-level inverters can be applied.

**2) Voltage/Current Control at DC Side:**

Define a control variable $v_{2X}$ as

$$v_{2X} = \frac{1}{2} (i_{P X} + i_{N X})$$

(5)

and circulating current $i_{Z X}$ flowing through both the upper and lower arms as

$$i_{Z X} = \frac{1}{2} (i_{P X} + i_{N X})$$

(6)

Substituting (5) and (6) into (1) yields

$$L \frac{\text{d} i_{P X}}{\text{d} t} + R i_{Z X} = \frac{1}{2} V_{dc} - v_{2X}$$

(7)

According to KCL

$$I_d = \sum i_{P X} = \sum i_{N X} = \frac{1}{2} \sum (i_{P X} + i_{N X}) = \sum i_{Z X}$$

(8)
3) Total Energy Control in Each Phase-Leg:
To maintain a constant average capacitor voltage during each fundamental period, the voltages or energies stored in the capacitors of each arm should be controlled properly. The internal energies of the arms shown below are chosen as dynamic control variables

\[
W_{CpX} = \sum_{j=1}^{N} \left( \frac{1}{2} C_{Cpj} v_{Cpj}^2 \right) = \frac{1}{2} C \sum_{j=1}^{N} v_{Cpj}^2
\]

\[
W_{Cnx} = \sum_{j=1}^{N} \left( \frac{1}{2} C_{Cnj} v_{Cnj}^2 \right) = \frac{1}{2} C \sum_{j=1}^{N} v_{Cnj}^2
\]

The total energy \((W \Sigma C_X)\) and the differential energy \((W \Delta C_X)\) in each phase-leg are

\[
W \Sigma C_X = W_{Cpx} + W_{Cnx}
\]

\[
W \Delta C_X = W_{Cpx} - W_{Cnx}
\]

Ignoring power losses, the power relationships are

\[
\frac{dW_{Cpx}}{dt} = \frac{1}{2} V_{dc} v_x - L \frac{di_{pX}}{dt} - R i_{pX} i_x
\]

\[
\frac{dW_{Cnx}}{dt} = \frac{1}{2} V_{dc} v_x - L \frac{di_{nX}}{dt} - R i_{nX} i_x
\]

Since to filter the switching frequency harmonics the inductors in each phase-leg are used, the ac-side voltage and current can be assumed to be sinusoidal

\[
\begin{aligned}
  v_x &= v_x \sin(\omega t) \\
  i_x &= I_x \sin(\omega t - \delta)
\end{aligned}
\]

\[
p \Sigma i_{Cx} = -2L \frac{di_{2x}}{dt} i_{2x}
\]

4) Differential Energy Control in Each Phase-Leg:
Derivation of the differential energy can be represented as

where \(p \Sigma A1C_x\) is the fundamental component of \(dW \Delta C_x\) d\(t\).

\[
i_{2x} = I_{1x} \sin(\omega t + \varphi_x)
\]

\[
p_{0cx} = I_{1x} \varphi_x - 2i_{2x} \cos(\varphi_x)
\]

\[
p_{0cx} = -v_x i_{1x} \cos(\varphi_x) - v_{dx} i_{2x}
\]

5) Overall Control Structure:
The total energy control, differential energy control, circulating current control, and ac current control are all included. Based on the aforementioned analyses, for MMC operating as an inverter an energy-based overall control structure is presented. To simplify the computation all burden, the capacitor voltages within one arm are supposed to be balanced, i.e.

\[
\begin{aligned}
W_{Cpx} &= \frac{1}{2} C \sum_{j=1}^{N} (v_{Cpj}^2) \\
W_{Cnx} &= \frac{1}{2} C \sum_{j=1}^{N} (v_{Cnj}^2)
\end{aligned}
\]

\[
\left\{ \begin{array}{l}
W_{Cpx} = \frac{1}{2} C \sum_{j=1}^{N} (v_{Cpj}^2) \\
W_{Cnx} = \frac{1}{2} C \sum_{j=1}^{N} (v_{Cnj}^2)
\end{array} \right.
\]

\[
\left\{ \begin{array}{l}
V_{px} = v_{2x} + v_{1x} \\
V_{px} = v_{2x} - v_{1x}
\end{array} \right.
\]

**IMPROVED MODULATION METHOD**

This paper proposes an improved PDPWM, which requires much less hardware comparing units, but can provide excellent performance with inherent voltage balancing. PDPWM is one of the most important modulation methods for MMC, using one voltage reference and a group of level shifted triangular carrier waves. However, powerful microcontroller chips with multiple modulation modules are required especially when the number of SMs is high, e.g., tens to hundreds.

In Fig. 4 the red dotted-line box indicates the closed-loop current control in applications like grid-connected converters. In the energy-based control structure in Fig. 4, Large signal models are used which guarantees large signal stability.
can be easily modified as shown in Fig. 5. Voltage-based control is more intuitive, but small-signal linearized models have to be used and large signal stability is difficult to guarantee at the controller design stage.

![Fig. 5. Modification from energy-based control into voltage-based control.](image)

Suppose the average value of the capacitor voltages in each arm is $V_c$, then the voltage reference $v$ can be separated into an integral part and a fractional part, as shown in (27)

$$v_n = (n-1)V_c + dV_c$$

(21)

Where $n = 1, 2, \ldots, N$, and $0 \leq d \leq 1$. That means, during each carrier period, only the $n$th SM operates in PWM mode (or switching mode), $(n-1)$ SMs (from 1 to $n-1$) at ON state, and $(N-n)$ SMs (from $n+1$ to $N$) at OFF state.

$$v_{\text{pwm}} = (n-1)V_c + v_p$$

(22)

![Fig. 6. Improved PDPWM with single reference and single carrier: (a) waveforms of reference and carrier; (b) implementation.](image)

![Fig. 7. Pulse distribution for PDPWM with four SMs in one arm: (a) expected pulse waveform; (b) direct pulse distribution; (c) proposed alternate pulse distribution.](image)

![Fig. 8. Flowchart of alternate pulse distribution (implemented in an FPGA).](image)
The proposed modulation method yields even distribution of switching frequency among power devices, which is similar to CPSPWM. The complexity and hardware cost of this algorithm are low and do not increase with the number of SMs. Nonetheless, the hardware cost of the proposed method is much lower since it does not need separate PWM comparator for each SM.

VOLTAGE BALANCING CONTROL

A new voltage balancing control method based on the improved PDPWM is presented in this paper, which does not need voltage sorting algorithm and does not cause extra switching actions.

The inherent voltage balancing capability of the improved PDPWM method is fairly good. However, some non-ideal factors, e.g., differences in the SMs’ losses and circuit parameters, can still disrupt the balance of capacitor voltages. Fig. 11 shows the control block diagram, where Δd is used for the computation of the time delay (Δt).

\[ \Delta d = \frac{\Delta T}{T_{cr}} \]  

Tcr is the carrier period. Thanks to the improved modulation method, a low bandwidth of the balancing control system can be selected. The upper limit of Δd in Fig. 10 can also be set to a low value, e.g., 10%.

Based on the assumption the comparison on cost is that the number of SMs within one arm is high. A comparison of present voltage balancing methods and the proposed method, which encompasses a broad range of features, is presented in Table I.

<table>
<thead>
<tr>
<th>Methods</th>
<th>BALANCING EFFICIENCY</th>
<th>DYNAMICS</th>
<th>INCLUDING FREQUENCY</th>
<th>AVERAGING</th>
<th>HARDWARE</th>
<th>SOFTWARE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposed method</td>
<td>High</td>
<td>Medium</td>
<td>Unchanged</td>
<td>No</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Reduced switching frequency</td>
<td>Medium</td>
<td>High</td>
<td>Increased</td>
<td>Yes</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Reduced switching frequency</td>
<td>Medium</td>
<td>Medium</td>
<td>Unchanged</td>
<td>No</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Other loop control</td>
<td>Low</td>
<td>Medium</td>
<td>Unchanged</td>
<td>No</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Other loop control</td>
<td>Medium</td>
<td>High</td>
<td>Increased</td>
<td>Yes</td>
<td>Low</td>
<td>Low</td>
</tr>
</tbody>
</table>

A. Proposed Voltage Balancing Control Scheme

In this paper, the balancing action is only applied to the SMs with the highest and lowest voltage, and the control algorithm is executed at a low frequency (fcr/N). In the improved PDPWM, the imbalance among capacitor voltages develops slowly, therefore at the switching frequency (fcr), the balancing control needs not to be executed and it needs not to adjust all the SMs. To satisfy the charge balance, if arm current is positive, the pulse width of the SM with highest voltage is reduced. The opposite thing happens when the arm current is negative while the pulse width of the SM with lowest voltage is increased by the same amount.

TABLE II: PARAMETERS OF THE THREE-PHASE MMC FOR SIMULATION

Fig. 11. Voltage balancing control within one arm.

Fig. 12. Capacitor voltages during start-up.
If the arm current is negative, the SM with the highest voltage is switched OFF with a delay, while the SM with the lowest voltage is switched ON with the same delay. This scheme can be realized as follows. First, in each carrier period, to find out the highest and lowest voltages the capacitor voltages are measured. If the arm current is positive, the SM with the highest voltage is switched ON with a delay ($\Delta t$), while the SM with the lowest voltage is switched OFF with the same delay.

**Fig. 13.** Capacitor voltages, upper/lower arm currents, and ac current in steadystate.

**Fig. 14.** Output voltages, output currents, arm currents, and capacitor voltage during sudden load changes.

**B. Selection of Time Delay $\Delta t$**

The difference ($\Delta vC$) between the highest voltage ($vC_{\text{max}}$) and lowest voltage ($vC_{\text{min}}$) is nearly constant, which should be zero when the voltage balancing is achieved. When the imbalance within one arm occurs, the average values of the capacitor voltages are different, but their low frequency ripples vary with the same amplitude and in the same direction. Therefore, $\Delta vC$ is used as the error and a simple P or PI controller is adopted to adjust the unbalance.

**C. Discussion**

To the original gating signals the proposed balancing method only adds delays, it does not cause unnecessary switching actions. Since the delays of the gating signals are the same, the volt-seconds of the arm voltages ($vP x$ and $vNx$) do not change during the time of $NTcr$. Therefore, the proposed method will not affect the converter output voltage. (which may occur with conventional module selection methods).

Compared with the method proposed so higher balancing accuracy can be achieved, since the control error in the proposed method is a dc component while the errors contain low-frequency ripples. To find out SMs with the highest and lowest voltages. The method avoids the usage of a full sorting algorithm since it only needs. Therefore, the computational burden is reduced, especially when the number of SMs is fairly high.

**Fig. 15.** Capacitor voltages, arm currents, and ac current with and without voltage balancing control.

**SIMULATION RESULTS**

To verify the proposed control system, a three-phase MMC inverter with a resistor-inductor load is developed by MATLAB/Simulink software, and the parameters are summarized in Table II. PI controllers are used for total energy control, differential energy control, and circulating current control in the simulations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>Rated active power, $P$</td>
<td>2 kW</td>
</tr>
<tr>
<td>Rated reactive power, $Q$</td>
<td>0.5 MVA</td>
</tr>
<tr>
<td>Line voltage (Vline), $E_{\text{line}}$</td>
<td>6 kV</td>
</tr>
<tr>
<td>Line-to-line frequency, $f_{\text{line}}$</td>
<td>50 Hz</td>
</tr>
<tr>
<td>SM capacitance, $C_{\text{cap}}$</td>
<td>0.15 mF</td>
</tr>
<tr>
<td>Arm equivalent capacitance, $C_{\text{eq}}$</td>
<td>0.25 mF</td>
</tr>
<tr>
<td>SM capacitance, $C_{\text{cap}}$</td>
<td>1 mF</td>
</tr>
<tr>
<td>Rated arm voltage, $E_{\text{arm}}$</td>
<td>2.2 kV</td>
</tr>
<tr>
<td>Switching frequency, $f_{\text{switch}}$</td>
<td>1 kHz</td>
</tr>
<tr>
<td>Equivalent switching frequency in one period, $f_{\text{equ}}$</td>
<td>6 kHz</td>
</tr>
</tbody>
</table>

**TABLE III: PARAMETERS OF THE THREE-PHASE MMC FOR EXPERIMENT**
CONCLUSION

A new method for voltage balancing among arm capacitors, which is based on an improved pulse-width modulation, is presented. It avoids some major disadvantages found in present voltage balancing methods, such as dependence on computation-intensive voltage sorting algorithms, extra switching actions, interference with output voltage, etc. The improved PDPWM method distributes the gating pulses alternately among the SMs within one arm every N (number of SMs within one arm) several carrier periods. Single reference and single carrier (for one arm) used in the modulation reduce the control hardware requirement. For medium-
high-voltage applications, these features make the proposed balancing control method a more suitable solution, where the number of SMs in each arm can be fairly high. A general-purpose control structure is also proposed, which is adaptable for various control modes. Simulation results verified the good performances of the MMC system with the proposed methods. The performances of the improved modulation and balancing control are found to be satisfactory except for some extreme cases where the SM switching frequency drops below 100 Hz. For both voltage-based and energy-based control methods a control structure for MMC inverters is presented in this paper, which is suitable, and includes voltage balancing between the upper and lower arms. By using the simulation results verify the effectiveness of the proposed methods.

REFERENCES


Fahad Bin Nahadi

Fahad Bin Nahadi received the Bachelor of Technology Degree in Electrical & Electronics Engineering from vijaya Krishna institute of technology and sciences affiliated to Jawaharlal Nehru Technological University, Hyderabad, India, in 2014. Currently, he is pursuing Master of technology in AL-Habeeb College of Engineering and Technology Under Jawaharlal Nehru Technological University, Hyderabad, India. He has published a number of papers in various national & international journals & conferences. His research areas are power electronics and FACTS.

Email id: fahad.nahdi1991@gmail.com

Sri. Vadla Chandra Shekhar

Sri. Vadla Chandra Shekhar received his Bachelor of Technology Degree in Electrical & Electronics Engineering from Jawaharlal Nehru Technological University, Hyderabad, India, 2012 & Master of Technology Degree in Electrical & Electronics Engineering from Jawaharlal Nehru Technological University, Hyderabad, India, in 2015. Currently, he is working as an Assistant Professor in Al-Habeeb College of Engineering and Technology, Chevella, Telangana, India. He has published a paper in international journals & conferences.
Co-guidance
Sri. Karimulla Peerla Shaik
received his Bachelor of Technology Degree in Electrical & Electronics Engineering from Jawaharlal Nehru Technological University, Hyderabad, India, 2006 & Master of Technology Degree in Electrical & Electronics Engineering from Jawaharlal Nehru Technological University, Hyderabad, India, in 2011. Currently, he is pursuing Ph.D from Jawaharlal Nehru Technological University, Kakinada, India, and working as an Associate Professor in Al-Habeeb College of Engineering and Technology, Chevella, Telangana, India. He has published a number of papers in various national & international journals & conferences. His research areas are power system economics and optimization.
Email: karim.02214@gmail.com