A HIGH STEP-UP THREE-PORT DC-DC CONVERTER FOR STAND-ALONE PV/BATTERY POWER SYSTEM WITH FUZZY CONTROLLER

CHITTIMURI APARNA
M.tech
QIS College of engineering & technology
Ongole, JNTUK (A.P).
E-Mail: appu.sri0209@gmail.com

SANGU RAVINDRA
Associate Professor
QIS College of engineering & technology
Ongole, JNTUK (A.P).
E-Mail: Sanguravindra11@gmail.com

Abstract— In this paper, we are using fuzzy logic controller for the control scheme of the proposed converter provides maximum utilization of PV power most of the time. The coupled inductors are used to achieve high step-up voltage gain and to reduce the voltage stress of input side switches. Two sets of active-clamp circuits are used to recycle the energy stored in the leakage inductors and to improve the system efficiency. Fuzzy logic controller having more advantages than the other controllers. The operation mode does not need to be changed when a transition between charging and discharging occurs. Moreover, tracking maximum power point of the PV source and regulating the output voltage can be operated simultaneously during charging/discharging transitions. A three-port dc–dc converter integrating photovoltaic (PV) and battery power for high step-up applications with grid connected mode is proposed in this paper. The topology includes five power switches, two coupled inductors, and two active-clamp circuits. As long as the sun irradiation level is not too low, the maximum power point tracking (MPPT) algorithm will be disabled only when the battery charging voltage is too high. As a result, the proposed converter has merits of high boosting level, reduced number of devices, and simple control strategy. Experimental results of a 200-W laboratory prototype are presented to verify the performance of the proposed three-port converter.

Key words – DC-DC converter, PV battery power system, Micro grid.

INTRODUCTION

Therefore, it is very important for the port connected to the energy storage to allow bidirectional power flow. Various kinds of topologies have been proposed due to the advantages of multiport converters. The combination strategies for the multiport converter include sharing switches, capacitors, inductors, or magnetic cores [1]. One could select a proper topology by considering many aspects such as cost, reliability, and flexibility depending on the applications. Integrated multiport converters for interfacing several power sources and storage devices are widely used in recent years.

Instead of using individual power electronic converters for each of the energy sources, multiport converters have the advantages including less components, lower cost, more compact size, and better dynamic performance. In many cases, at least one energy storage device should be incorporated. For example, in the electric vehicle application, the regenerative energy occurs during acceleration or startup.

Fig. 1. Part of the FREEDM system diagram showing an SST-enabled DC microgrid.

An application of hybrid energy supply using renewable energy sources and storage devices is shown in Fig. 1. The dc microgrid enabled by the solid-state transformer (SST) in the Future Renewable Electric Energy Delivery and Management System (FREEDM System) integrates various distributed renewable energy resources (DRERs) and distributed energy storage devices (DESDs) [2]. For instance, if solar power is selected as the renewable energy source and battery as the storage device, the battery can either supply the load with the solar energy at the same time or store the...
excess power from the solar panels for backup use. Therefore, the bidirectional power path must be provided for the battery port. The dc–dc converters interfacing the DRERs or DESDs are expected to have relative high voltage conversion ratios since the dc bus of the FREEDM system is 380 V. It is studied that for the dc–dc converters connected to the solar panels, voltage gain extension cells such as coupled inductors, transformers, and switched capacitors are often employed to achieve high voltage conversion ratios [3]. By utilizing the voltage gain extension cells, the extreme duty cycles that exist in typical boost converters can be avoided and the voltage stress on switches can be reduced. Thus, power switches with lower voltage rating and lower turn-on resistance can be chosen for the converters to reduce conduction losses. A converter using coupled inductors is relatively better than isolation transformers since the coupled inductors have simpler winding structure and lower conduction loss [4]. However, the leakage inductors of the coupled inductors will consume significant energy for a large winding ratio. In such case, the voltage stress and the loss of the switches will both be increased. A boost converter with coupled inductor and active-clamp circuit is proposed in [4]. This boost converter can yield a high step-up voltage gain, reduce the voltage stress on switches, and recycle the energy in the leakage inductor.

Therefore, the system cost and volume can be reduced. The major contribution of this paper is to propose an integrated three-port converter as a non isolated alternative other than typical isolated topologies for high step-up three-port applications. The proposed switching strategy allows the converter to be controlled by the same two duty cycles in different operation modes.

II. PRINCIPLE OF OPERATION

This section introduces the topology of proposed non isolated three-port dc–dc converter, as illustrated in Fig. 2. The converter is composed of two main switches $S_1$ and $S_2$ for the battery and PV port. Synchronous switch $S_3$ is driven complementarily to $S_1$ such that bidirectional power flow for the battery port can be achieved. Two coupled inductors with winding ratios $n_1$ and $n_2$ are used as voltage gain extension cells. Two sets of active clamp circuits formed by $S_4$, $Lk_1$, $Cc_1$ and $S_5$, $Lk_2$, $Cc_2$ are used to recycle the leakage energy. $Lk_1$ and $Lk_2$ are both composed of a small leakage inductor from the coupled inductor and an external leakage inductor. Two independent control variables, duty cycles $d_1$ and $d_2$ , allow the control over two ports of the converter, while the third port is for the power balance. The fixed-frequency driving signals of the auxiliary switches $S_3$ and $S_4$ are complementary to primary switch $S_1$ . Again, $S_3$ provides a bidirectional path for the battery port. Similarly, $S_5$ is driven in a complementary manner to $S_2$ . A 180 ° phase shift is applied between the driving signals of $S_1$ and $S_2$.

There are four operation periods based on the available solar power. First, the sun is in the eclipse stage and the solar irradiation is either unavailable or very low. This operation period is defined as period 1, and the battery will serve as the main power source. As the sun starts to shine and the initial solar irradiation is enough for supplying part of the load demand, the operation period is changed to period 2. The load is supplied by both solar and battery power in this period. For period 3, the increasing isolation makes the solar power larger than the load demand. The battery will preserve extra solar power for backup use. During period 4, the charging voltage of the battery reaches the preset level and should be limited to prevent overcharging. According to the solar irradiation and the load demand, the proposed three-port converter can be operated under two modes. In the battery balance mode (mode 1), maximum power point tracking (MPPT) is always operated for the PV port to draw maximum power from the solar panels. The battery port will maintain the power balance by storing the unconsumed solar power during light-load condition or providing the power deficit during heavy-load condition. The power sharing of the inputs can be represented as

$$P_{load} = P_{pv\ SVC} + P_{bat\ SVC} \quad (1)$$

where $P_{load}$ is the load demand power, $P_{pv\ SVC}$ is the PV power under solar voltage control (SVC), and $P_{bat\ SVC}$ is the battery power under SVC. In mode 1, maximum power is drawn from the PV source. The battery may provide or absorb power depending on
the load demand. Therefore, $P_{\text{bat SVC}}$ could be either positive or negative. When the battery charging voltage is higher than the maximum setting, the converter will be switched into battery management mode (mode 2). In mode 2, MPPT will be disabled; therefore, only part of the solar power is drawn. However, the battery voltage could be controlled to protect the battery from overcharging. The power sharing of the inputs can be represented as

$$P_{\text{load}} = P_{\text{pv BVC}} + P_{\text{pv BVC}}$$

where $P_{\text{pv BVC}}$ is the PV power under battery voltage control (BVC) and $P_{\text{bat BVC}}$ is the battery charging power under SVC. If the load is increased and the battery voltage is reduced, the converter will be switched to mode 1. The output voltage is always kept at 380 V in both modes.

### III. TOPOLOGICAL MODES AND ANALYSIS

#### A. PV Source Modeling

It is well explained in the literature [29]–[32] that using a PV generator as input source has significant effect on the converter dynamics. The nonlinear $V-I$ characteristic of a PV generator can be modeled using current source, diode, and resistors. The single-diode model shown in Fig. 3(a) is widely used for the PV source modeling. This model provides a tradeoff between accuracy and complexity [33]. Thevenin’s equivalent model with non constant voltages and resistances has been proposed in [35]–[38] to closely approximate the characteristic of PV generator. The Thevenin-based model provides simpler prediction and computation for the maximum power point of PV array under different operating conditions.

Thevenin’s theorem is not valid for a nonlinear model, but the nonlinear model could be represented by a linear one with non constant parameters [36]. In [37], for example, the piecewise linearization is used to linearize the diode. The parameters in Fig. 3(a) can be estimated using the manufacturer’s datasheet [39]. As shown in Fig. 3(b), the actual diode characteristic has been divided into three regions and the characteristic in each region is approximated as a straight line. Each line can be further represented by a set of voltage source $V_{x,n}$ and resistance $R_{D,n}$ ($n = 1,2,3$). The approximation of piecewise linearization would be more accurate as the number of regions increased. At the boundary points of regions, the values of linearized characteristic are exactly the same as actual characteristic. Therefore, the maximum power point of the PV generator is chosen as one of the boundary points such that the operation at this point has no approximation error.

Fig. 3. Thevenin’s equivalent circuit derived from the single-diode model. (a) Single-diode model of a PV generator. (b) $V-I$ characteristic of diode: actual and linear approximation [34]. (c) Single-diode model with linearized diode. (d) Thevenin’s equivalent circuit for a single-diode model with linearized diode.
From the derivation in [35], the \( V_{pvth} \) and \( R_{pvth} \) can be calculated by

\[
V_{pvth,n} = V_{X,n} + R_{D,n} \frac{R_{sh} I_{ph} - V_{n}}{R_{sh} + R_{D,n}}
\]

\[
R_{pvth,n} = R_g + \frac{R_{sh} R_{D,n}}{R_{sh} + R_{D,n}}
\]

For the following discussion, the Thevenin’s equivalent model is adopted for the PV generator modeling.

**B. Operation of the Topological Modes**

Before performing the analysis, some assumptions should be made: 1) the switches are assumed to be ideal; 2) the magnetizing inductors are large enough so that the current flowing through the inductors is constant; 3) the capacitors are large enough so that the voltages across the capacitors are constant.

The topological modes over a switching cycle are shown in Fig. 4 and key waveforms of the proposed converter are given in Fig. 5. Detailed explanation of each interval is given as follows:

**Interval 1** [see Fig. 4(a), \( t_0 \leq t < t_1 \)]: At \( t_0 \), switches \( S_4 \) and \( S_5 \) are turned OFF, while primary switch \( S_2 \) is turned ON. Although \( S_1 \) is in the off state, resonant inductor \( L_{k1} \) resonates with \( C_{r1} \) and \( C_{r4} \). In this period, \( C_{r1} \) is discharged to zero and \( C_{r4} \) is charged to \( V_{bat} + V_{C_{c1}} \). For the PV port, \( S_2 \) is turned ON and the current from the PV panels flows through \( V_{pv} - L_2 - L_{k2} - S_2 \) loop. In order to achieve the ZVS feature for \( S_1 \), the energy stored in resonant inductor \( L_{k1} \) should satisfy the following inequality:

\[
L_{k1} \geq \frac{(C_{r1} |I_{DS1}|^2 I_{DS1}(t_0))^2}{|I_{DS1}(t_0)|^2}
\]

**Interval 2** [see Fig. 4(b), \( t_1 \leq t < t_2 \)]: This mode starts when \( v_{ds1} \) is down to zero. The body diode of \( S_1 \) is forward biased so that the ZVS condition for \( S_1 \) is established. The resonant current \( i_{L_{k1}} \) is increased toward zero. \( L_2 \) is still linearly charged in this period.

**Interval 3** [see Fig. 4(c), \( t_2 \leq t < t_3 \)]: \( S_1 \) begins to conduct current at \( t_2 \) and the battery port current follows the path \( V_{bat} - L_1 - L_{k1} - S_1 \). \( S_2 \) is also turned ON in this interval. Therefore, both \( L_1 \) and \( L_2 \) are linearly charged and energy of both input ports is stored in these magnetizing inductors. Auxiliary switches \( S_3, S_4, \) and \( S_5 \) are all turned OFF.

**Interval 4** [see Fig. 4(d), \( t_3 \leq t < t_4 \)]: In this interval, \( S_2 \) starts to be turned OFF and the auxiliary switch \( S_5 \) remains in the OFF state. However, a resonant circuit formed by \( L_{k2}, C_{r2} \), and \( C_{r5} \) releases the energy stored in \( L_{k2} \). Resonant capacitor \( C_{r2} \) is quickly charged to \( V_{pv} + V_{C_{c2}} \) while \( C_{r5} \) is discharged to zero. In order to achieve the ZVS feature for \( S_5 \), the energy stored in resonant inductor \( L_{k2} \) should satisfy the following.
Fig. 4. Topological modes of the proposed converter. (a) Interval 1. (b) Interval 2. (c) Interval 3. (d) Interval 4. (e) Interval 5. (f) Interval 6. (g) Interval 7. (h) Interval 8. (i) Interval 9. (j) Interval 10. (k) Interval 11. (l) Interval 12.

Fig. 5. Key waveforms of the proposed converter inequality:
Interval 5 [see Fig. 4(e), t4 ≤ t < t5]: At t4, vDS5 reaches zero and the body diode across the auxiliary switch S5 is turned ON. Therefore, a ZVS condition for S5 is established. Given that the C r5 is much smaller than C r2, almost all of the magnetizing currents are recycled to charge the clamp capacitor C r2. Furthermore, VC c2 is considered as a constant value since the capacitance of C r2 is large enough. This interval ends when inductor current iLk2 drops to zero.

\[ L_{k2} \geq \frac{[C_{r1}][C_{r5}]|v_{DS5}(t_5)|^2}{\bar{i}_{Lk2}(t_5)^2} \]  

(6)

Interval 6 [see Fig. 4(f), t5 ≤ t < t6]: At t5, the current of Lk2 is reversed in direction and energy stored in i5 is released through the Cr2 – S5 – Lk2 – L3 loop. This interval ends when S5 is turned OFF.

Interval 7 [see Fig. 4(g), t6 ≤ t < t7]: Switches S2 and S5 are both in the OFF state at t6. A resonant circuit is formed by Lk2, Cr2, and Cr5. During this interval, Cr2 is discharged to zero and C r5 is charged to VpVth + VCc2. To ensure the ZVS switching of S2, the energy stored in Lk2 should be greater than the energy stored in parasitic capacitors Cr2 and Cr5.

\[ L_{k2} \geq \frac{[C_{r1}][C_{r5}]|v_{DS2}(t_6)|^2}{\bar{i}_{Lk2}(t_6)^2} \]  

(7)

Interval 8 [see Fig. 4(h), t7 ≤ t < t8]: This interval starts when the voltage across Cr2 is zero and the body diode DS2 is turned ON. Leakage inductor current iLk2 is linearly increased and the secondary-current of the coupled inductor is increased as well. The main switch S2 should be turned ON before iLk2 becomes positive to ensure ZVS operation.

Interval 9 [see Fig. 4(i), t8 ≤ t < t9]: The circuit operation of interval 9 is identical to interval 3 since S1 and S2 are turned ON in both intervals.

Interval 10 [Fig. 4(j), t9 ≤ t < t10]: At t9, S1 is turned OFF, while S3 and S4 remain in OFF state. During this interval, Lk1 will resonate with Cr1 and Cr4 to release the energy trapped in it. Resonant capacitor Cr1 is charged to Vbat + VC c1, while Cr 4 is discharged to zero. To achieve the ZVS feature for S4, the energy stored in resonant inductor Lk2 should satisfy the following inequality:

\[ L_{k1} \geq \frac{v_{DS1}^2(C_{r1}[C_{r4}])}{i_{DS1,peak}^2} \]  

(8)

Interval 11 [see Fig. 4(k), t10 ≤ t < t11]: This interval begins when vDS4 drops to zero and the body diode across S4 is turned ON. The ZVS condition for S4 is then established. Almost all of the magnetizing current is recycled to charge Cc1 since Cr4 is much smaller than Cr1. Moreover, VC c1 is considered as a constant value since the capacitance of Cc1 is large enough. This interval ends when inductor current iLk1 reaches zero. Interval 12 [see Fig. 4(l), t11 ≤ t < t12]: The current flow through Lk1 is reversed in direction at t11, and the energy stored in Cc1 is released through the Cc1 – S4 – Lk1 – L1 loop. This interval ends when S4 is turned OFF and the operation of the proposed converter over a switching cycle is complete.

A.ZVS Analysis

According to the (5)–(8), ZVS at turn-on transition could be achieved when enough energy is stored in the leakage inductors Lk1 and Lk2. The ZVS conditions for switches S1 – S4 should be determined by (5) and (7) since the ZVS transient periods of S1 and v are less than that of S4 and S5. The voltages across switches S1 and S2 can be expressed as

\[ v_{DS1} = V_{bat} + V_{Cc1} \]  

(9)

\[ v_{DS2} = V_{pV,th} + V_{Cc2} \]  

(10)

The peak current flow through S1 and S2 can be obtained as

\[ i_{DS1,peak} = \frac{v_{DS1}}{t_{d1}} + \frac{V_{DS1}}{t_{d2}} \]  

(11)

\[ i_{DS2,peak} = \frac{v_{DS2}}{t_{d1}} + \frac{V_{DS2}}{t_{d2}} \]  

(12)

where \( \eta \) represents the converter efficiency. It is noted that as long as Lk1 and Lk2 are both in the OFF state at t6. Moreover, leakage inductor: Lk1 = L1 and Lk2 = L2, the behavior of the converter duty cycle is approximately the same as for the non active clamp converter in the continuous conduction mode. Typically, Lk1 = L1 /10 and Lk2 = L2 /10 can be the conservative design guidelines. The effective duty cycles delf1 and delf2 are assumed to be equal to d1 and d2 for subsequent equations. As a result, the following inequalities can be derived from (9)–(12) to determine a proper leakage inductance:

\[ L_{k1} \geq \frac{v_{DS1}^2(C_{r1}[C_{r4}])}{i_{DS1,peak}^2} \]  

(13)

\[ L_{k2} \geq \frac{v_{DS2}^2(C_{r2}[C_{r5}])}{i_{DS2,peak}^2} \]  

(14)

IV.MODELING AND CONTROL STRATEGY

As mentioned in Section II, the operation modes of the converter are determined by the conditions of available solar power and battery charging states. Controlling the converter in each mode requires different state variables to regulate voltages of the input and output ports. There are three control loops for the proposed converter: output voltage control (OVC), SVC, and BVC. The control scheme is shown in Fig. 6. The OVC is a simple voltage regulation loop. The SVC and BVC loops share the same control variable \( d2 \) to achieve smooth
mode transitions. SVC is used to regulate the voltage of the PV port and implement the MPPT algorithm. BVC is the battery voltage regulation loop to prevent overcharging. It is noted that the PV port is operated under SVC most of the time. Therefore, BVC would not be active under normal operation. Only one control loop between SVC and BVC is performed. Moreover, once BVC starts to take control over \( d_2 \), SVC will be disabled immediately to avoid the noise issue caused by the MPPT algorithm [27]. In fact, the cross-coupled control loops is the intrinsic feature of the multiport converters since it is a high-order system. It will be a challenge to design the controllers of a multiport converter. The decoupling network for extracting separate transfer functions in such a system has been introduced by describing the system dynamics in a matrix form [23].

![Fig. 6. Control scheme of the proposed three-port converter.](image)

![Fig. 7. Steady-state waveforms of the three-port converter.](image)

The small-signal modeling method is widely used for the power electronics converter. For a three-port converter that has two input ports, a matrix-form model will be very helpful to implement the closed-loop control and analyze the system dynamics. Since there are two operation modes for the proposed three-port converter, two sets of small-signal models will be derived. The state variables for each model are slightly different but the control variables are the same. The decoupling network is required for both models to allow separate controller design.

**A. Small-Signal Modeling in Battery Balance Mode**

Four state variables including magnetizing inductor currents \( iL1 \) and \( iL2 \), PV port voltage \( vC2 \), output voltage \( vO \) are selected to derive the small-signal model in this mode. From Fig. 7, a switching cycle can be divided into four main circuit stages depending on the ON–OFF state of the two main switches. A set of state equations can be developed for each stage based on Kirchhoff’s Current Law and Kirchhoff’s Voltage Law.

- **Switching state 1 \([0 \leq t < (1-(1-d_2))Ts/2]\):** At \( t = 0 \), primary switches \( S1 \) and \( S2 \) are turned ON and auxiliary switches \( S3, S4 \), and \( S5 \) are turned OFF. Inductors \( L1 \) and \( L2 \) are both charged and the power from the input ports is stored in the magnetizing inductors. The state equations can be represented in

\[
\begin{align*}
L_1 \frac{di_{L1}}{dt} &= v_{c1} \\
L_2 \frac{di_{L2}}{dt} &= v_{c2} \\
C_2 \frac{dv_{C2}}{dt} &= i_{L2} - \frac{(v_{pv.th} - v_{C2})}{R_{pv.th}} \\
C_0 \frac{dv_{C0}}{dt} &= -\frac{v_{c0}}{R}
\end{align*}
\]

- **Switching state 2 \([(d1-(1-d_2))Ts/2 \leq t < (d1+(1-d_2))Ts/2]\):** At \( t = (d1-(1-d_2))Ts/2 \), switches \( S1 \) and \( S3 \) are turned ON and switches \( S2, S3 \), and \( S4 \) are turned OFF. Therefore, inductor \( L1 \) is still charged but inductor \( L2 \) is discharged

\[
\begin{align*}
L_1 \frac{di_{L1}}{dt} &= v_{c1} \\
L_2 \frac{di_{L2}}{dt} &= -\frac{n_1v_{C1} - v_{C0}}{n_2} \\
C_2 \frac{dv_{C2}}{dt} &= -\frac{(v_{pv.th} - v_{C2})}{R_{pv.th}} \\
C_0 \frac{dv_{C0}}{dt} &= \frac{i_{L2} - v_{C0}}{n_2} - \frac{v_{C0}}{R}
\end{align*}
\]

- **Switching state 3 \([(d1+(1-d_2))Ts/2 \leq t < d1Ts]\):** At \( t = (d1+(1-d_2))Ts/2 \), switches \( S1 \) and \( S2 \) are turned ON and switches \( S3, S4 \), and \( S5 \) are turned OFF. Thus, inductors \( L1 \) and \( L2 \) are both charged again as in switching state 1

\[
\begin{align*}
L_1 \frac{di_{L1}}{dt} &= v_{c1} \\
L_2 \frac{di_{L2}}{dt} &= v_{c2} \\
C_2 \frac{dv_{C2}}{dt} &= i_{L2} - \frac{(v_{pv.th} - v_{C2})}{R_{pv.th}} \\
C_0 \frac{dv_{C0}}{dt} &= -\frac{v_{C0}}{R}
\end{align*}
\]
Switching state $4 \{d1Ts \leq t < Ts \}$: At $t = d1 \ Ts$, switches S2, S3, and S4 are turned ON and switches S1 and S5 are turned OFF. Inductors $L1$ is discharged but inductor $L2$ is charged

\[
\begin{align*}
L_1 \frac{di_{L1}}{dt} &= \frac{C_1}{1-d_1} - \frac{n_2 v_{c2} - v_0}{n_1} \\
L_2 \frac{di_{L2}}{dt} &= v_{c2} \\
C_2 \frac{dv_{c2}}{dt} &= \frac{n_2}{n_1} i_{L1} + i_{L2} - \frac{(v_{pv th} - v_{C2})}{R_{pv th}} \\
C_0 \frac{dv_{C0}}{dt} &= \frac{i_{L1} - v_0}{n_1} - \frac{v_0}{n_2}
\end{align*}
\]

(18)

Using the volt–second balance and current–second balance theory [28], the state-space averaged equations can be obtained using (15)–(18)

\[
\begin{align*}
L_1: d_1 T_s v_{C1} + (1 - d_1) T_s &\frac{v_{c1}}{1-d_1} - \frac{n_2 v_{c2} - v_0}{n_1} = 0 \\
&\Rightarrow v_0 = \frac{1-n_2 d_1}{1-d_1} v_{c1} - n_2 v_{C2} \\
L_2: d_2 T_s v_{C2} + (1 - d_2) T_s &\frac{-n_1 v_{C1} - v_0}{n_2} = 0 \\
&\Rightarrow v_0 = -n_1 v_{C1} + n_2 \frac{d_2}{1-d_2} v_{C2}
\end{align*}
\]

(20)

Using the averaged signal model with decoupling network

\[
A = \begin{bmatrix}
0 & 0 & \frac{n_2 (1-D_1)}{n_1} & \frac{(1-D_1)}{L_1} \\
0 & 0 & \frac{n_2}{n_1} & \frac{L_2}{(1-D_2)} \\
\frac{n_2 (1-D_2)}{n_1 C_0} & \frac{D_2}{C_2} & \frac{1}{R_{pv th C_2}} & 0 \\
\frac{(1-D_1)}{n_1 C_0} & \frac{(1-D_2)}{n_1 C_0} & 0 & \frac{1}{RC_0}
\end{bmatrix}
\]

(21)

Using this model, the transfer functions for the PV port voltage and output port voltage to the duty cycle values of the main switches could be obtained based on the small-signal diagram shown in Fig. 8. For the system of proposed converter, the state variables are controlled by two control variables. The transfer function matrix can be represented as

\[
G = C(sI - A)^{-1}B + D
\]

(27)

where \(x\) represents the state variable vector containing \(iL1, iL2, vC2\), and \(v0, u\) represents the control variable vector containing \(d1\) and \(d2\), and \(y\) represents the output variable vector. In this case, the four state variables are also the system output. The small-signal model can be described as

Using this model, the transfer functions for the PV port voltage and output port voltage to the duty cycle values of the main switches could be obtained based on the small-signal diagram shown in Fig. 8. For the system of proposed converter, the state variables are controlled by two control variables. The transfer function matrix can be represented as

\[
G = C(sI - A)^{-1}B + D
\]

(27)

where \(G(jk)\) represents the transfer function of \(j\)th state variable to the \(k\)th control variable. These transfer functions can be calculated using the computer software such as MATLAB and are not presented because of their complexity. In order to design the closed-loop compensators separately, a decoupling network is introduced to decouple the interactive control loops [23].
B. Small-Signal Modeling in Battery Manage Mode
The small-signal model in battery manage mode can be derived by the same method. However, in this mode, the battery port voltage $v_{C1}$ is considered as one of the state variables instead of the PV port voltage $v_{C2}$. The four state variables are now $i_{L1}, i_{L2}, v_{C1}$, and $v_{0}$, while the control variables are still $d_{1}$ and $d_{2}$. The state-space averaged model in this mode could be represented as

![Diagram of small-signal model with decoupling network and compensators in the battery manage mode.](Fig. 9)

Using equations (29) and (33), the system compensators could be designed with desired bandwidth, phase margin, and steady state error. For the proposed converter, an integration unit should be incorporated to eliminate the steady-state error of the system step responses. Although the steady-state error could be eliminated by adding an integral unit, the bandwidth would be reduced and may lead the system to be unstable. To achieve proper phase margin of $60^\circ \leq \text{P.M.} \leq 90^\circ$ and enough bandwidth, a lead unit should also be included in addition to the integral unit since the integral unit will lower the cutoff frequency and decrease the phase margin. The bandwidth of the BVC and SVC could be designed to be about one decade lower than OVC to achieve tight load regulation.

V. FUZZY LOGIC CONTROLLER
In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC. The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani’s, ‘min’ operator. v. Defuzzification using the height method.

**Fuzzification:** Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The partition of fuzzy subsets and the shape of membership function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor.

![Diagram of fuzzy logic controller partition and membership function.](Fig. 6)

<table>
<thead>
<tr>
<th>Change in error</th>
<th>Error</th>
</tr>
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<tbody>
<tr>
<td>NB</td>
<td>PB</td>
</tr>
<tr>
<td>NM</td>
<td>PB</td>
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In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular $E(k)$ input there is only one dominant fuzzy subset. The input error for the FLC is given as

$$E(k) = \frac{P_{ph(k)} - P_{ph(k-1)}}{V_{ph(k)} - V_{ph(k-1)}}$$

**Table I Fuzzy Rules**

Using equations (29) and (33), the system compensators could be designed with desired bandwidth, phase margin, and steady state error. For the proposed converter, an integration unit should be incorporated to eliminate the steady-state error of the system step responses. Although the steady-state error could be eliminated by adding an integral unit, the bandwidth would be reduced and may lead the system to be unstable. To achieve proper phase margin of $60^\circ \leq P.M. \leq 90^\circ$ and enough bandwidth, a lead unit should also be included in addition to the integral unit since the integral unit will lower the cutoff frequency and decrease the phase margin. The bandwidth of the BVC and SVC could be designed to be about one decade lower than OVC to achieve tight load regulation.
CE(k) = E(k) – E(k-1)

Fig.7. Membership functions

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

Defuzzification: As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height” method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error and output.

The set of FC rules are derived from

\[ u = \alpha E + (1 - \alpha)C \]

Where \( \alpha \) is self-adjustable factor which can regulate the whole operation. \( E \) is the error of the system, \( C \) is the change in error and \( u \) is the control variable. A large value of error \( E \) indicates that given system is not in the balanced state. If the system is unbalanced, the controller should enlarge its control variables to balance the system as early as possible. One the other hand, small value of the error \( E \) indicates that the system is near to balanced state. Overshoot plays an important role in the system stability. Less overshoot is required for system stability and in restraining oscillations. During the process, it is assumed that neither the UPQC absorbs active power nor it supplies active power during normal conditions. So the active power flowing through the UPQC is assumed to be constant. The set of FC rules is made using Fig.(b) is given in Table 1.

VI. SIMULATION RESULTS
Fig. 15. Measured waveforms of load step response under SVC (Ch1: Vo, Ch2: Io, Ch3: Ipv, Ch4: Ib).

(a) 

(b) 

Fig. 16. Autonomous mode transition. (a) Mode 1 to mode 2. (b) Mode 2 to mode 1 (Ch1: Vo, Ch2: Vb, Ch3: Ipv, Ch4: Ipv)

VII. CONCLUSION

In the proposed topology, two coupled inductors are employed as voltage gain extension cells for high voltage output applications. A high step-up three-port DC–DC converter for grid connected systems is proposed to integrate solar and battery power by using fuzzy logic controller. The proposed switching strategy only needs to control two duty ratios in different operation modes. The experimental results validate the functionality of the proposed converter under different solar irradiation level and load demand. Fuzzy logic controller reduces the THD value in the prescribed limits. Two sets of buck–boost type active-clamp circuits are used to recycle the energy stored in the leakage inductors and improve the efficiency. The charging/discharging transitions of the battery could be achieved without changing the operation mode; therefore, the MPPT operation will not be interrupted. In light-load condition, once the charging voltage is higher than the preset level, the operation mode will be changed rapidly to protect the battery from overcharging. The highest converter efficiency is measured as 90.1% at 110 W.

REFERENCES