DESIGN AND ANALYSIS OF FIVE-LEVEL INVERTER FOR RENEWABLE POWER GENERATION SYSTEM

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Abstract—In this paper we propose better solution for designing five-level inverter by injecting small amount of real power from the renewable power source into the grid to consistently reduce the switching power loss, the harmonic distortion in it, and EMI in power electronic devices caused by switching operation. In order to construct we require 2 dc capacitors, full-bridge inverter, a dual buck converter and filter. Here role of dual-buck converter is to converts 2 dc capacitor voltage sources to a dc output voltage with three levels and that balances these 2 dc capacitor voltages, thus output voltage of dual-buck converter supplies to full-bridge inverter. Finally it is designed to produce output current controlled to generate a sinusoidal current in phase with utility voltage to inject to grid. A hardware prototype is developed to verify the performance of the developed renewable power generation system. The experimental results show that the developed renewable power generation system reaches the expected performance.

Index Terms—Harmonic distortion, inverters, power electronics.

I. INTRODUCTION

The Demand for renewable energy has increased significantly over the years because of shortage of fossil fuels and greenhouse effect. The definition of renewable energy includes any type of energy generated from natural resources that is infinite or constantly renewed. Examples of renewable energy include solar, wind, and hydropower. Renewable energy, due to its free availability and its clean and renewable character, ranks as the most promising renewable energy resources like Solar energy, Wind energy that could play a key role in solving the worldwide energy crisis.

The conventional single-phase inverter topologies for grid connection include half-bridge and full bridge [1]–[4]. The half-bridge inverter is configured by one capacitor arm and one power electronic arm. The dc bus voltage of the half-bridge inverter must be higher than double of the peak voltage of the output ac voltage. The output ac voltage of the half-bridge inverter is two levels. The voltage jump of each switching is the dc bus voltage of the inverter. The full-bridge inverter is configured by two power electronic arms. The popular modulation strategies for the full-bridge inverter are bipolar modulation and unipolar modulation [3], [5]–[7].

In this paper we propose better solution for designing five-level inverter by injecting small amount of real power from the renewable power source into the grid to consistently reduce the switching power loss, the harmonic distortion in it, and EMI in power electronic devices caused by switching operation. In order to construct we require 2 dc capacitors, full-bridge inverter, a dual buck converter and filter. Here role of dual-buck converter is to converts 2 dc capacitor voltage sources to a dc output voltage with three levels and that balances these 2 dc capacitor voltages, thus output voltage of dual-buck converter supplies to full-bridge inverter. Finally it is designed to produce output current controlled to generate a sinusoidal current in phase with utility voltage to inject to grid. A hardware prototype is developed to verify the performance of the developed renewable power generation system. The experimental results show that the developed renewable power generation system reaches the expected performance.

The common three topologies for multilevel inverters are as follows:

1) Diode clamped (neutral clamped).
2) Capacitor clamped
3) Cascaded H-bridge inverter.

A multilevel inverter is power conversion device that produces an output voltage in the needed levels by using DC voltage sources applied to input [3]. Multilevel inverter which performs power conversion by using the discrete DC voltage sources was firstly introduced in 1975, this multilevel inverter structure consists of the H-bridges connected in series. Then, the diode-clamped multilevel inverter was emerged. It employs the capacitors connected in series to separate the DC bus voltage in different levels. In 1992, the capacitor clamped multilevel inverter was introduced. This structure is similar to the structure of the diode-clamped multilevel inverter, but it uses the capacitors instead of the diodes to clamp the voltage levels.

Multilevel inverter can effectively reduce the voltage jump of each switching operation to reduce the switching loss and increase power efficiency. The number of power electronic switches used in the multilevel inverter is larger than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is more complicated. Thus, both the performance and complexity should be considered in designing the multilevel inverter [8], [9]. However, interest in the multilevel inverter has been aroused due to its advantages of better power efficiency, lower
In this paper, a five-level inverter is developed and applied for injecting the real power of the renewable power into the grid. This five-level inverter is configured by two dc capacitors, a dual-buck converter, a full-bridge inverter, and a filter [22]. The five-level inverter generates an output voltage with five levels and applies in the output stage of the renewable power generation system to generate a sinusoidal current in phase with the utility voltage to inject into the grid. The power electronic switches of the dual-buck converter are switched in high frequency to generate a three-level voltage and balance the two input dc voltages. The power electronic switches of the full-bridge inverter are switched in low frequency synchronous with the utility to convert the output voltage of the dual-buck converter to a five-level ac voltage. Therefore, the switching power loss, harmonic distortion, and electromagnetic interference (EMI) caused by the switching operation of power electronic devices can be reduced, and the control circuit is simplified. Besides, the capacity of output filter can be reduced. A hardware prototype is developed to verify the performance of the developed renewable power generation system.

II. CIRCUIT CONFIGURATION

As conventional single-phase multilevel inverter topologies include the diode-clamped, the flying capacitor, and the cascade H-bridge types as shown in Fig. 1. Fig. 1(a) is the basic configuration of a diode-clamped multilevel inverter. Where it is configured by 2 dc capacitors, two diodes, and 4 power electronic switches.

Two diodes are used to conduct the current loop, and four power electronic switches are used to control the voltage levels. The output voltage of the basic diode-clamped multilevel inverter has three levels. The control for balancing these two dc capacitors is very important.

Fig. 1(b) shows the circuit configuration of a basic flying capacitor multilevel inverter. As can be seen, it is configured by three dc capacitors and four power electronic switches. If five-level output voltage is required, an extra dc capacitor and four power electronic switches are required.

Fig. 1(c) shows the circuit configuration of the basic cascade H-bridge multi-level inverter. As can be seen, it is configured by two full-bridge inverters connected in cascade. However, this topology has the disadvantages that two independent dc voltage sources are required.

Fig. 2 shows the circuit configuration of the five-level inverter applied to a photovoltaic power generation system. As can be seen, it is configured by a solar cell array, a dc–dc converter, a five-level inverter, two switches, and a digital signal processor (DSP)-based controller. Switches SW1 and SW2 are placed between the five-level inverter and the utility, and they are used to disconnect the photovoltaic power generation system from the utility when islanding operation occurs. The load is placed between switches SW1 and SW2.

Fig. 3 shows the operation modes of this five-level inverter. As can be seen, the power electronic switches of the full-bridge inverter are switched in low frequency and synchronously with the utility voltage to convert the dc power into ac power for commutating. As seen in Fig. 3(a)–(d), the power electronic switches S1 and S7 are in the ON state, and the power electronic switches S8 and S6 are in the OFF state during the positive half-cycle. On the contrary, the power electronic switches S1 and S7 are in the OFF state, and the power electronic switches S8 and S6 are in the ON state during the negative half-cycle. Since the dc capacitor voltages Vc2 and Vc3 are balanced by controlling the five-level inverter, the dc capacitor voltages Vc2 and Vc3 can be represented as follows:

$$V_{c2} = V_{c3} = \frac{1}{3} V_d_c.$$  \hspace{1cm} (1)

The operation modes of this five-level inverter are stated as follows.
Mode 1: Fig. 3(a) shows the operation circuit of mode 1. The power electronic switch of the dual-buck converter $S_2$ is turned ON and $S_3$ is turned OFF. DC capacitor $C_2$ is discharged through $S_2$, $S_4$, the filter inductor, the utility, $S_7$, and $D_3$ to form a loop. Both output voltages of the dual-buck converter and five-level inverter are $V_{dc}/2$.

Mode 2: Fig. 3(b) shows the operation circuit of mode 2. The power electronic switch of the dual-buck converter $S_2$ is turned OFF and $S_3$ is turned ON. DC capacitor $C_3$ is discharged through $D_2$, $S_4$, the filter inductor, the utility, $S_7$, and $S_8$ to form a loop. Both output voltages of the dual-buck converter and five-level inverter are $V_{dc}/2$.

Mode 3: Fig. 3(c) shows the operation circuit of mode 3. Both power electronic switches $S_2$ and $S_3$ of the dual-buck converter are turned OFF. The current of the filter inductor flows through the utility, $S_7$, $D_3$, $D_2$, and $S_4$. Both output voltages of the dual-buck converter and five-level inverter are 0.

Mode 4: Fig. 3(d) shows the operation circuit of mode 4. Both power electronic switches $S_2$ and $S_3$ of the dual-buck converter are turned ON. DC capacitors $C_2$ and $C_3$ are discharged together through $S_2$, $S_4$, the filter inductor, the utility, $S_7$, and $S_8$ to form a loop. Both output voltages of the dual-buck converter and five-level inverter are $V_{dc}$.

Modes 5–8 are the operation modes for the negative half-cycle. The operations of the dual-buck converter under modes 5–8 are similar to that under modes 1–4, and the dual-buck converter can also generate three voltage levels $V_{dc}/2$, $V_{dc}/2$, 0, and $V_{dc}$, respectively. However, the operation of the full-bridge inverter is the opposite. The power electronic switches $S_4$ and $S_8$ are in the OFF state, and the power electronic switches $S_6$ and $S_8$ are in the ON state during the negative half-cycle. Therefore, the output voltage of the five-level inverter for modes 5–8 will be $-V_{dc}/2$, $-V_{dc}/2$, 0, and $-V_{dc}$, respectively.

Considering operation modes 1–8, the full-bridge inverter converts the dc output voltage of the dual-buck converter with three levels to an ac output voltage with five levels which are $V_{dc}$, $V_{dc}/2$, 0, $-V_{dc}/2$, and $-V_{dc}$. The operation of power electronic switches $S_2$ and $S_3$ should guarantee the output voltage of the dual-buck converter is higher than the absolute of the utility voltage. The waveforms of output voltage of five-level inverter and utility voltage are shown in Fig. 4.

![Fig. 4. Waveforms of output voltage and utility voltage.](image)

**Fig. 5. Equivalent circuit. (a) $|v_s| < V_{dc}/2$. (b) $|v_s| > V_{dc}/2$.**

<table>
<thead>
<tr>
<th>$V_{C2} &gt; V_{C3}$</th>
<th>$S_2$</th>
<th>$S_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM</td>
<td>off</td>
<td>PWM</td>
</tr>
<tr>
<td>$V_{C2} &lt; V_{C3}$</td>
<td>$S_2$</td>
<td>$S_3$</td>
</tr>
<tr>
<td>off</td>
<td>PWM</td>
<td>on</td>
</tr>
</tbody>
</table>

Table 1 ON/OFF State of $S_2$ and $S_3$

Due to the operation of full-bridge inverter, the voltage and current in the dc side of full-bridge inverter are their absolute values of the utility voltage and the output current of the five-level inverter. When the absolute of the utility voltage is smaller than $V_{dc}/2$, the output voltage of the dual-buck converter should change between $V_{dc}/2$ and 0. Accordingly, the power electronics of five-level inverter is switched between modes 1 or 2, and mode 3 during the positive half-cycle. On the contrary, the power electronics of five-level inverter is switched between modes 5 or 6, and mode 7 during the negative half-cycle. One of the power electronic switches $S_2$ and $S_3$ is in the OFF state and the other is switched in high frequency during one PWM period. Fig. 5(a) shows the equivalent circuit for the dc side of the five-level inverter under $|v_s| < V_{dc}/2$. As seen in Fig. 5(a), the equivalent circuit is a conventional buck converter. DC voltage source $V_{dc}$ may be dc capacitor voltage $V_{C2}$ or $V_{C3}$, and it depends on which power electronic switch $S_2$ or $S_3$ is switching in high frequency. As the power electronic switch is turned ON, the change rate of the output current can be represented as follows:
(2) where \( L \) is the inductance of the filter inductor. The change rate of the output current is positive. Thus, the output current \( |i_o| \) increases when the power electronic switch is turned ON. As the power electronic switch is turned OFF, the change rate of the output current can be represented as follows:

\[
\frac{d|io|}{dt} = \frac{V_{dc} - |v_s|}{L}
\]

(3)
The change rate of the output current is negative, meaning the output current \( |i_o| \) will decrease when the power electronic switch is turned OFF. As seen in (2) and (3), the output current \( |i_o| \) can be controlled by the ON/OFF operation of the power electronic switch to track a reference current signal.

When the absolute of the utility voltage is higher than \( V_{ac}/2 \), the output voltage of the dual-buck converter should be changed between \( V_{ac} \) and \( V_{ac}/2 \). Accordingly, the five-level inverter is operated in mode 4, and 1 or 2 during the positive half-cycle, and it is switched in modes 5, 8, and 8 or 6 during the negative half-cycle. One of power electronic switches \( S_2 \) and \( S_3 \) is still turned ON and the other is switched in high frequency during one PWM period. Fig. 5(b) shows the equivalent circuit for the dc side of the five-level inverter under \( |v_s| > V_{ac}/2 \). The dc voltage source \( V_{dc} \) is the summation of dc capacitor voltages \( V_{C2} \) and \( V_{C3} \). As seen in Fig. 5(b), it differs from the conventional buck inverter, where voltage source \( V_{dc} \) is connected to the diode in series. Voltage source \( V_{dc} \) may be dc capacitor voltage \( V_{C2} \) or \( V_{C3} \), and it depends on which power electronic switch \( S_3 \) or \( S_2 \) is switched in high frequency. As the power electronic switch is turned ON, the change rate of the output current can be represented as follows:

\[
\frac{d|io|}{dt} = \frac{V_{dc} - |v_s|}{L}
\]

(4)
The change rate of the output current \( |i_o| \) is positive, meaning the output current \( |i_o| \) increases when the power electronic switch is turned ON. As the power electronic switch is turned OFF, the change rate of the output current can be represented as follows:

\[
\frac{d|io|}{dt} = \frac{V_{dc} - |v_s|}{L}
\]

(5)
The change rate of the output current \( |i_o| \) is negative, and the output current \( |i_o| \) inductor current will be decreased when the power electronic switch is turned OFF. As seen in (4) and (5), the output current \( |i_o| \) can also be controlled to track a reference current signal by controlling the ON/OFF operation of the power electronic switches under \( |v_s| > V_{ac}/2 \).

Hence, the output current of the five-level inverter can be controlled to track a reference current signal, which is a sinusoidal current in phase with the utility voltage by controlling the ON/OFF operation of the power electronic switches \( S_2 \) and \( S_3 \). Meanwhile, the five-level inverter will generate a five-level output voltage varying with the change of the utility voltage. The switching loss, filter inductor, and EMI are reduced because the voltage difference of each voltage level is only \( V_{ac}/2 \).

IV. VOLTAGE BALANCE OF FIVE-LEVEL INVERTER

Balancing the voltages of dc capacitors is very important in controlling the multilevel inverter. The voltage balance of dc capacitor voltages \( V_{C2} \) and \( V_{C3} \) can be controlled by the power electronic switches \( S_2 \) and \( S_3 \) easily. When the absolute of the utility voltage is smaller than \( V_{ac}/2 \), one power electronic switch either \( S_2 \) or \( S_3 \) is switched in high frequency and the other is still in the OFF state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages \( V_{C2} \) and \( V_{C3} \). If dc capacitor voltage \( V_{C2} \) is higher than dc capacitor voltage \( V_{C3} \), power electronic switch \( S_3 \) is switched in high frequency. In this situation, the voltage source \( V_{C3} \) in Fig. 5(a) is \( -V_{C3} \), and \( C_3 \) will be discharged. Thus, the dc capacitor voltages \( V_{C2} \) decreases and \( V_{C3} \) does not change. On the contrary, power electronic switch \( S_2 \) is switched in high frequency when voltage \( V_{C3} \) is higher than voltage \( V_{C2} \). In this situation, the voltage source \( V_{C3} \) in Fig. 5(a) is \( V_{C2} \). Thus, the dc capacitor voltages \( V_{C2} \) decreases and \( V_{C3} \) does not change. In this way, the voltage balance of \( C_2 \) and \( C_3 \) can be achieved.

When the absolute of the utility voltage is higher than \( V_{ac}/2 \), one power electronic switch either \( S_2 \) or \( S_3 \) is switched in high frequency and the other is still in the ON state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages \( V_{C2} \) and \( V_{C3} \). If dc capacitor voltage \( V_{C2} \) is higher than dc capacitor voltage \( V_{C3} \), the power electronic switch \( S_3 \) is switched in high frequency. The voltage source \( V_{C3} \) in Fig. 5(b) is \( V_{C2} \). When the power electronic switch \( S_3 \) is turned ON, both \( C_2 \) and \( C_3 \) are discharged. However, only \( C_2 \) supplies the power when the power electronic switch \( S_3 \) is turned OFF. Thus, \( C_2 \) will discharge more power than that of \( C_3 \). On the contrary, the power electronic switch \( S_2 \) is switched in high frequency when dc capacitor voltage \( V_{C2} \) is higher than dc capacitor voltage \( V_{C3} \). The voltage source \( V_{C2} \) in Fig. 5(b) is \( dc \) capacitor voltage \( V_{C2} \). When the power electronic switch \( S_2 \) is turned ON, both \( C_2 \) and \( C_3 \) are discharged. However, only \( C_2 \) supplies the power when the power electronic switch \( S_2 \) is turned OFF. Thus, \( C_2 \) will discharge more power than that of \( C_3 \). In this way, the voltage balance of \( C_2 \) and \( C_3 \) can be achieved.

As mentioned earlier, the operation of power electronic switches \( S_2 \) and \( S_3 \) can be summarized as Table I. The voltages of capacitors \( C_2 \) and \( C_3 \) can be easily balanced compared with the conventional multilevel inverter.

V. CONTROL BLOCK DIAGRAM

Fig. 6 shows the control block diagram of five-level inverter. In the operation of the five-level inverter, the dc bus
voltage must be regulated to be larger than the peak voltage of the utility, and the dc capacitor voltages of $C_2$ and $C_3$ must be controlled to be equal. Besides, the five-level inverter must generate a sinusoidal current in phase with the utility voltage to be injected into the utility. As seen in Fig. 6, the voltages of dc capacitors $C_2$ and $C_3$ are detected and then added to obtain a dc bus voltage $V_{ac}$. The added result is subtracted from a dc bus setting voltage $V_{ac set}$. The dc bus setting voltage $V_{ac set}$ is larger than the peak voltage of the utility. The subtracted result is sent to a P-I controller. An islanding detection is also incorporated into the control of the five-level inverter. The concept of this islanding detection was proposed by authors [23]. However, it will not be addressed in this paper. As seen in Fig. 6, the utility current is detected and sent to an RMS detection circuit. The output of the RMS detection circuit is sent to a hysteresis comparator that contains a low threshold value and a high threshold value. If the RMS value of the utility current is smaller than the low threshold value, the output of the hysteresis comparator is high, meaning the condition of islanding operation or power balance occurs. On the contrary, the output of the hysteresis comparator is low when the RMS value of the utility current is larger than the high threshold value, meaning the utility is normal. The output of the hysteresis comparator is sent to a signal generator. The output signal of the signal generator is an islanding control signal $S_a$. The islanding control signal is a dc signal with unity amplitude if the output of the hysteresis comparator is low. On the contrary, the islanding control signal is a square wave with a frequency of 20 Hz (disturbance signal for islanding detection) when the output of the hysteresis comparator is high. The outputs of the PI controller and signal generator are sent to a multiplier, and the product of the multiplier is the amplitude of the reference signal. The utility voltage is detected and then sent to a phase-lock loop (PLL) circuit to generate an unity-amplitude sinusoidal signal whose phase is in phase with the utility voltage. The outputs of the multiplier and the PLL circuit are sent to the other multiplier. The product of this multiplier is the reference signal of the output current for the five-level inverter. The output current of the five-level inverter is detected by a current sensor. The reference signal and detected inductor current are sent to a subtractor. The subtracted result is sent to a current-mode controller. The output of the current-mode controller is sent to a PWM circuit to generate a PWM signal. The detected dc capacitor voltages $V_{cz}$ and $V_{cz}$ are also sent to a comparator to obtain signal $S_c$. When dc capacitor voltage $V_{cz}$ is higher than dc capacitor voltage $V_{cz}$, $S_c$ is a high value. On the contrary, $S_c$ is a low value when dc capacitor voltage $V_{cz}$ is smaller than dc capacitor voltage $V_{cz}$. DC voltage $V_{ac}$ is also sent to an amplifier with a gain of 0.5 to obtain voltage signal $V_{ac}/2$. The detected utility voltage is sent to an absolute circuit to obtain voltage signal $|V_s|$. Voltage signals $V_{ac}/2$ and $|V_s|$ are compared to obtain signal $S_e$. When $V_{ac}/2 > |V_s|$, $S_e$ is a high value. On the contrary, $S_e$ is a low value when $V_{ac}/2 < |V_s|$. The output signal of the PWM circuit and signals $S_a$ and $S_e$ are sent to the mode selection circuit. The output of the mode selection circuit will generate the control signals of power electronic switches $S_2$ and $S_3$. The detected utility voltage is also sent to a comparator to obtain complementary square signals that are synchronous with the detected utility voltage. The complementary square signals are the control signals of the power electronic switches of the full-bridge inverter. As mentioned earlier, only two power electronic switches $S_2$ or $S_3$ in the five-level inverter should be switched in high frequency, and only one of them is switched in high frequency at any time, and the voltage level of every switching is $V_{ac}/2$. Therefore, the five-level inverter can reduce the switching loss effectively.

![Fig.7. Control block diagram of five-level inverter.](image)

A ripple voltage with a frequency double that of the utility will appear in the dc bus voltage $V_{ac}$, while the five-level inverter injects real power into the utility. The function of MPPT will be degraded, while the output voltage of solar cell array contains a ripple voltage. Therefore, the ripple voltage superimposed on the dc bus voltage $V_{ac}$ must be blocked by the dc–dc converter for improving the function of MPPT. Accordingly, the dual control loops, an outer voltage control loop, and an inner current control loop are applied to control the dc–dc converter. Since the output voltage of the dc–dc converter is the dc bus voltage that is controlled to be a constant voltage by the five-level inverter, the outer voltage control loop is used to regulate the output voltage of the solar cell array. The inner current control loop is applied to control the inductor current to approach a constant current to block the ripple voltage of dc bus voltage $V_{ac}$. The output power of the solar cell array is calculated from the product of the output voltage of the solar cell array and the inductor current. Therefore, the output voltage of the solar cell array and the inductor current are detected and sent to a MPPT controller to determine the desired output voltage of the solar cell array. The detected output voltage and desired output voltage of the solar cell array are sent to a subtractor, and the subtracted result is sent to a P-I controller. The output of the P-I controller is the reference signal of the inner current control loop. The reference signal and the detected inductor current

![Diagram](image)
are sent to a subtractor, and the subtracted result is sent to an amplifier to complete the inner current control loop. The output of the amplifier is sent to the PWM circuit. The output signal of the PWM circuit is the driving signal for the power electronic switch of the dc-dc converter.

For protecting the renewable power generation system from the voltage rise, the MPPT function will be disabled and the power electronic switch $S_1$ will be turned OFF when the inverter stage is interrupted after detecting the islanding operation. Therefore, the output voltage of solar cell array is limited to the open-circuit voltage of solar cell array, and the dc bus voltage $V_{dc}$ is also limited.

Fig. 7. Control block of the dc–dc converter.

<table>
<thead>
<tr>
<th>Solar module</th>
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<th>DC–DC converter</th>
<th></th>
<th>DC–DC converter</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Rate of maximum power</td>
<td>75W</td>
<td>Capacitor ($C_1$)</td>
<td>470μF</td>
<td>Inductor ($L_1$)</td>
<td>2mH</td>
</tr>
<tr>
<td>Open voltage</td>
<td>21.7V</td>
<td>Switch frequency</td>
<td>5A</td>
<td>Switch frequency (PWM)</td>
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<tr>
<td>Short current</td>
<td>5.0A</td>
<td>Filter inductor ($L_f$)</td>
<td>1.4mH</td>
<td>DC bus setting voltage</td>
<td>110V</td>
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<tr>
<td>DC bus capacitor ($C_2$ and $C_3$)</td>
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<td>Switch frequency (PWM)</td>
<td>20kHz</td>
<td>Utility voltage</td>
<td>110V</td>
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<tr>
<td>Five-level inverter</td>
<td></td>
<td>DC capacitor voltage $V_{C_2}$</td>
<td></td>
<td>Utility frequency</td>
<td>60Hz</td>
</tr>
</tbody>
</table>

Table II Major parameters used in the experiment

VI. EXPERIMENTAL RESULTS

To verify the performance of the photovoltaic power generation system using the five-level inverter, a prototype based on the DSP controller of TMS320LF2407 A is developed and tested. The main parameters of the prototype are listed in Table II. The solar cell array consists of two strings, and each string contains eight solar modules connected in series. The capacity of solar cell array is 1.2 kW.
Fig. 8 shows the experimental results for the five-level inverter used in the developed photovoltaic power generation system under the steady state. The output power of the solar cell array is about 830 W. As seen in Fig. 8(b), the output current of the five-level inverter is sinusoidal and in phase with the utility voltage. The total harmonic distortion (THD%) of the utility voltage and the output current of the five-level inverter are 4.1% and 3.3%, respectively. As seen in Fig. 8(c) and (d), both dc capacitor voltages $V_{C2}$ and $V_{C3}$ remain in balance, and their voltage is about 85 V, respectively. Therefore, the dc bus voltage is regulated at 170 V. This verifies the five-level inverter can perform the functions of converting solar power to ac power with unity power factor, low THD%, and balancing two dc capacitor voltages effectively.

Since dc capacitors $C_2$ and $C_3$ perform the function of energy buffers, both dc capacitor voltages $V_{C2}$ and $V_{C3}$ contain a 120-Hz voltage ripple. Fig. 8 shows the experimental results for the dc–dc converter of the developed photovoltaic power generation system. Fig. 9(a) and (b) show the peak-to-peak value of the voltage ripple at dc capacitors $C_2$ and $C_3$ is about 7 V. As seen in Fig. 9(c), the peak-to-peak value of the voltage ripple at the solar cell array is only about 1.6 V. Fig. 8(d) shows the ripple of the inductor current is very small due to the use of the current mode control. In this way, the output voltage of the solar cell array can be more stable. This verifies that the developed control method for the dc–dc converter of the developed photovoltaic power generation system can effectively block the voltage ripple of five-level inverter delivering to the output voltage of the solar cell array.

Fig. 10 shows the experimental results for the full-bridge inverter of the five-level inverter. As can be seen, the input current $i_o$ of the full-bridge inverter shown in Fig. 10(b) is the absolute of the output current of the full-bridge inverter shown in Fig. 9(a). As seen in Fig. 10(c) and (d), the switch frequency of the power electronic switches $S_4$ and $S_5$ is 60 Hz. This verifies the power electronic switches of the full-bridge inverter are switched in low frequency, and the full-bridge inverter can convert the dc power into ac power by commutating.

Fig. 11 shows the experimental voltage of the five-level inverter. As seen in Fig. 11(c), the dual-buck converter outputs a dc voltage with three levels $V_a$, $V_a/2$, and 0. Fig. 11(b) shows the output voltage of the dual-buck converter is further converted to an ac voltage with five voltage levels $V_a$, $V_a/2$, 0, $-V_a/2$, and $-V_a$ by the full-bridge inverter. The voltage variation of each level is $V_a/2$. This verifies that the five-level inverter can generate a five-level output ac voltage according to the utility voltage and only the power electronic switches of the dual-buck converter is switched in high frequency.

**VII. CONCLUSION**

The developed five-level inverter can perform the functions of regulating the dc bus voltage, converting solar power to ac power with sinusoidal current and in phase with the utility voltage, balancing the two dc capacitor voltages, and detecting islanding operation. The experimental results verify the developed photovoltaic power generation system, and the five-level inverter achieves the expected performance.

**REFERENCES**


